

Compal Confidential

B5W18/19 Schematics Document

AMD "Carrizo/Carrizo-L/Bristol Ridge/Stoney Ridge" Platform

AMD 12~25W APU With Excavator/Puma+ Core

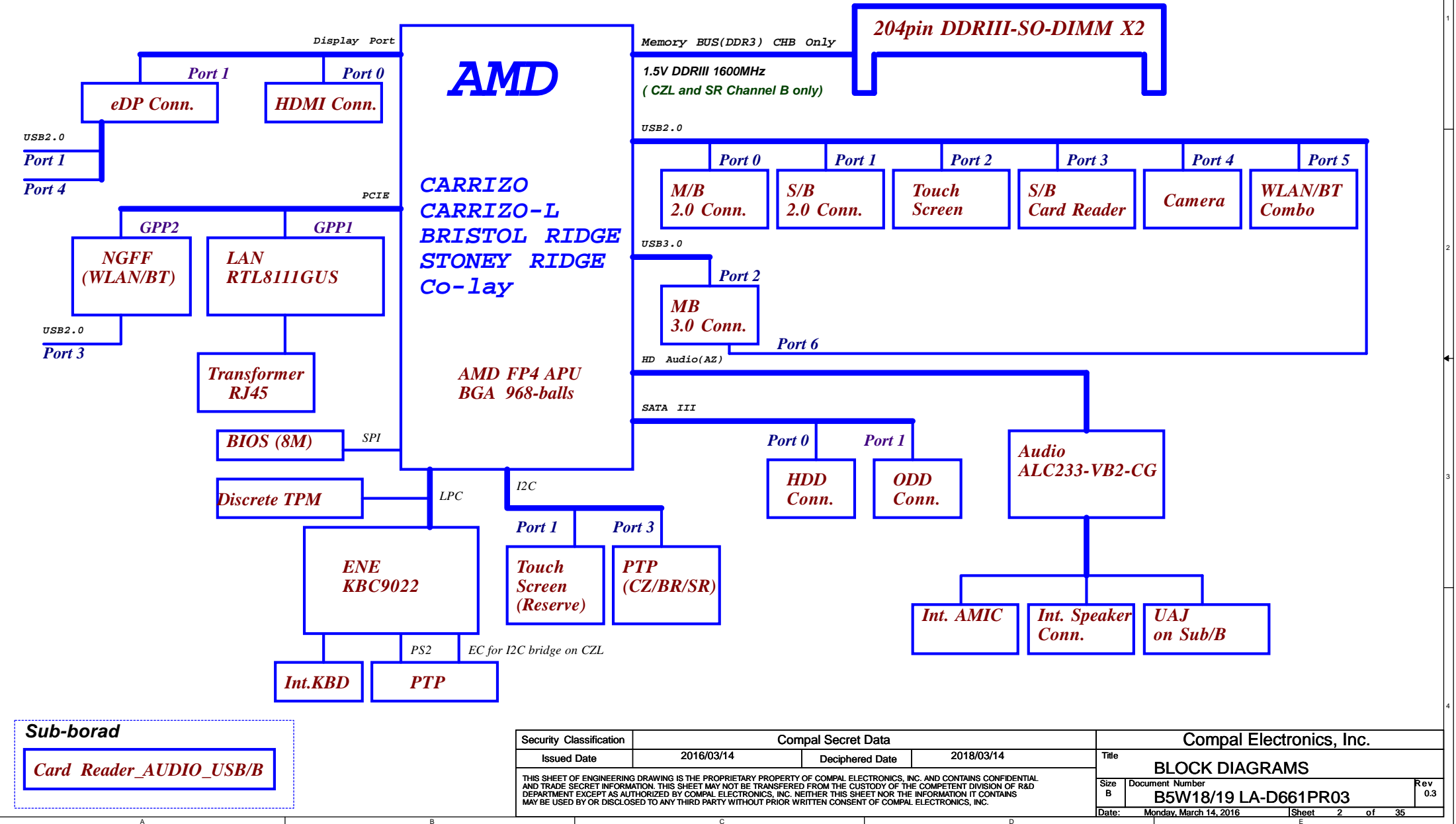
LA-D661P REV:0.3

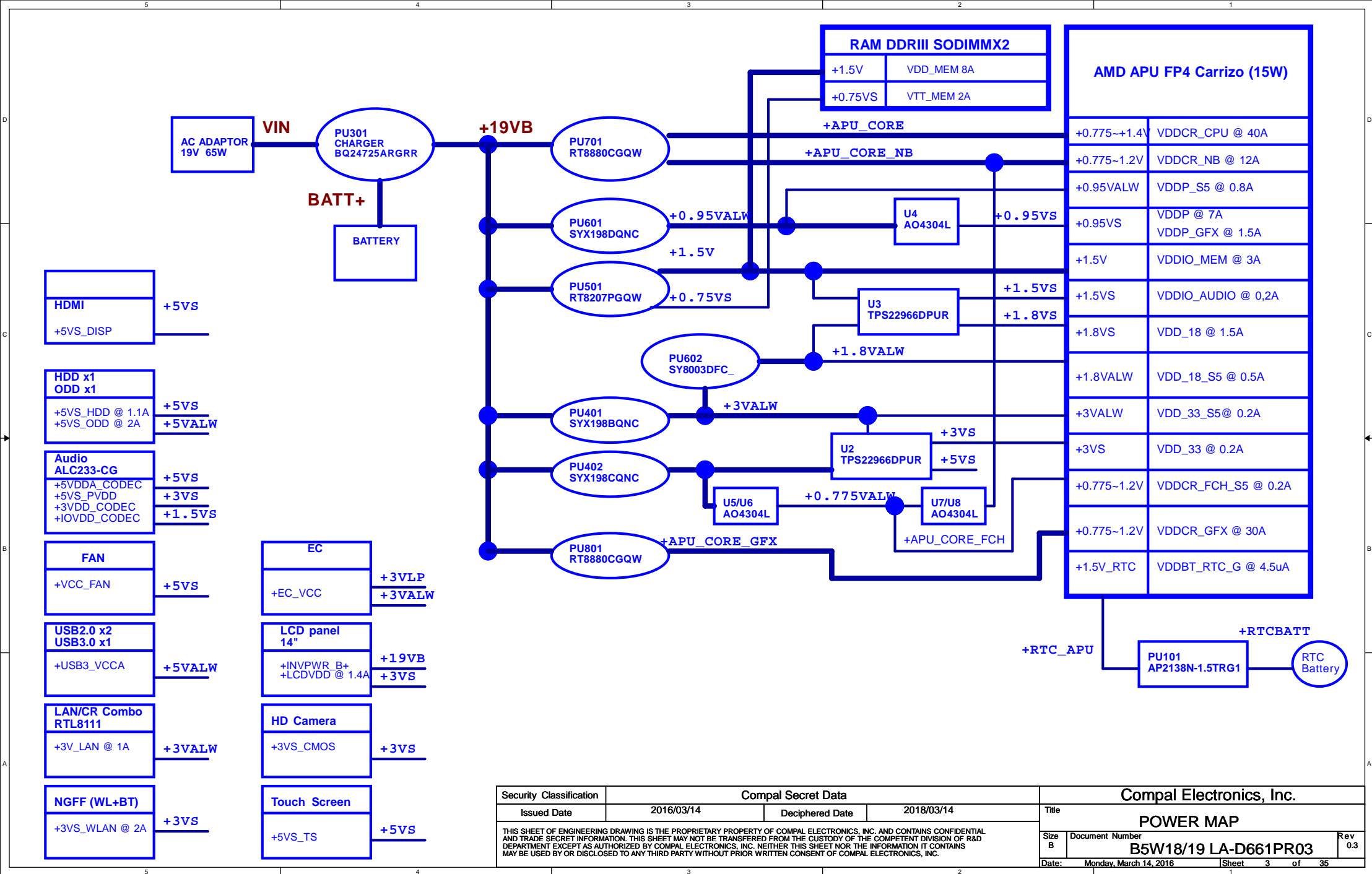
2016-03-14

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Model Name : Tricera_BS





Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+APU_CORE_GFX	Voltage for GFX	ON	OFF	OFF
+APU_CORE_FCH	Fusion Controller Hub Power Supply	ON	ON	ON
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+0.775VALW	0.775V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+0.95VSDGPU	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF

Master	Device	Address(7 bit)	Address(8bit)	
			Write	Read
APU SMBus Port 0 (+3VS)	JDIMM1	0101 0000b 50H	1010 0000b A0H	1010 0001b A1H
	JDIMM2	0101 0001b 51H	1010 0010b A2H	1010 0011b A3H
APU SMBus Port 1 (+3VALW)	Use As I2C			
APU I2C Port 0 (+1.8VS)	N.A			
APU I2C Port 1 (+1.8VS)	N.A			
APU I2C Port 2 (+3VS)	Use As SMBus			
APU I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2CH	0101 1000b 58H	0101 1001b 59H
EC SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0BH	0001 0110b 16H	0001 0111b 17H
	Charger IC (BQ24725)	0000 1001b 09H	0001 0010b 12H	0001 0011b 13H
EC SMBus Port 2 (+3VS)	APU Temp. (TSI)	0100 1100b 4CH	1001 1000b 98H	1001 1001b 99H

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOM Structure	BTO Item
@	Unpop
@EMC@	EMI/ESD Unpop
EMC@	EMI/ESD pop
T13EMC@	Carrizo/Bristol/Stoney EMI/ESD pop
T2EMC@	Carrizo-L EMI/ESD pop
255@	ALC255 Pop
233@	ALC233 Pop
9012@	KBC9012 Pop
9022@	KBC9022 Pop
T13@	Carrizo/Bristol/Stoney Pop
T1@	Carrizo/Bristol Pop
T2@	Carrizo-L Pop
T3@	Stoney Pop
8111H@	8111H Pop
8111GUS@	8111GUS Pop
TPM@	TPM Pop
45@	HDMI Royalty
CONN@	ME Connector
JP@	Jump
RS@	R-Short
TP@	Test Point
CZ@	BIOS Board ID for CZ
BR@	BIOS Board ID for BR

The diagram shows the timing of several signals relative to a common time axis. The signals are grouped into five categories: G-A, G-B, G-C, G-D, and G-E. Each category has a bracket on the left indicating its group. The signals are as follows:

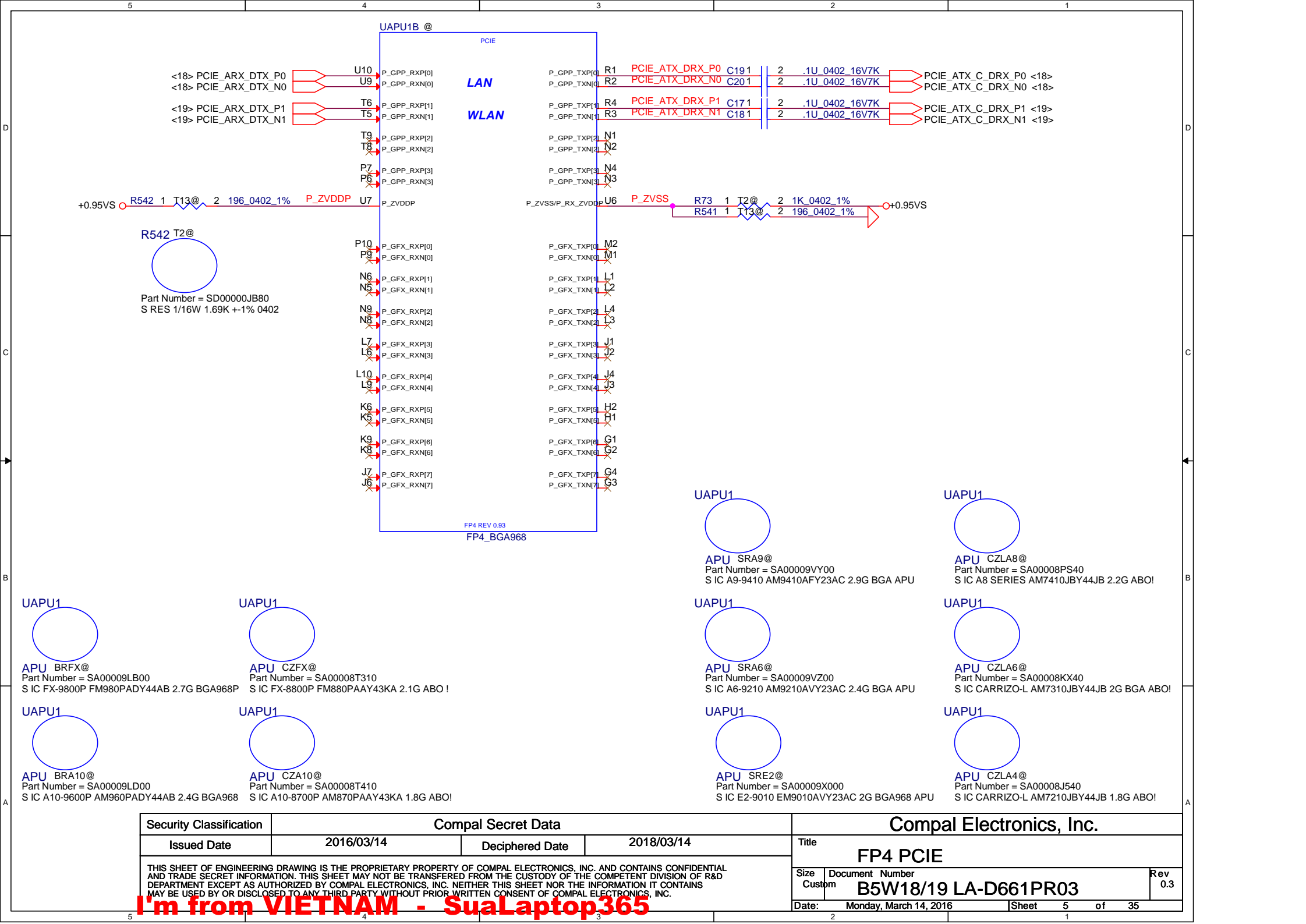
- G-A:**
 - +RTC
 - EC_ON
 - +5VALW
 - 3V_EN
 - +3VALW
 - 0.95_1.8VALW_PWREN
- G-B:**
 - +1.8VALW/+0.95VALW
 - 0.95V_SPOK
 - +0.775VALW
- G-C:**
 - SYSON
 - +1.5V
- G-D:**
 - SUSP#
 - +5VS/+3VS/+1.8VS
 - +1.5VS/0.75VS
 - 0.95VS_PWR_EN#
 - +0.95VS
- G-E:**
 - VR_ON
 - +APU_CORE
 - +APU_CORE_NB
 - +APU_GFX
- ZZZ:** A single signal represented by a circle.

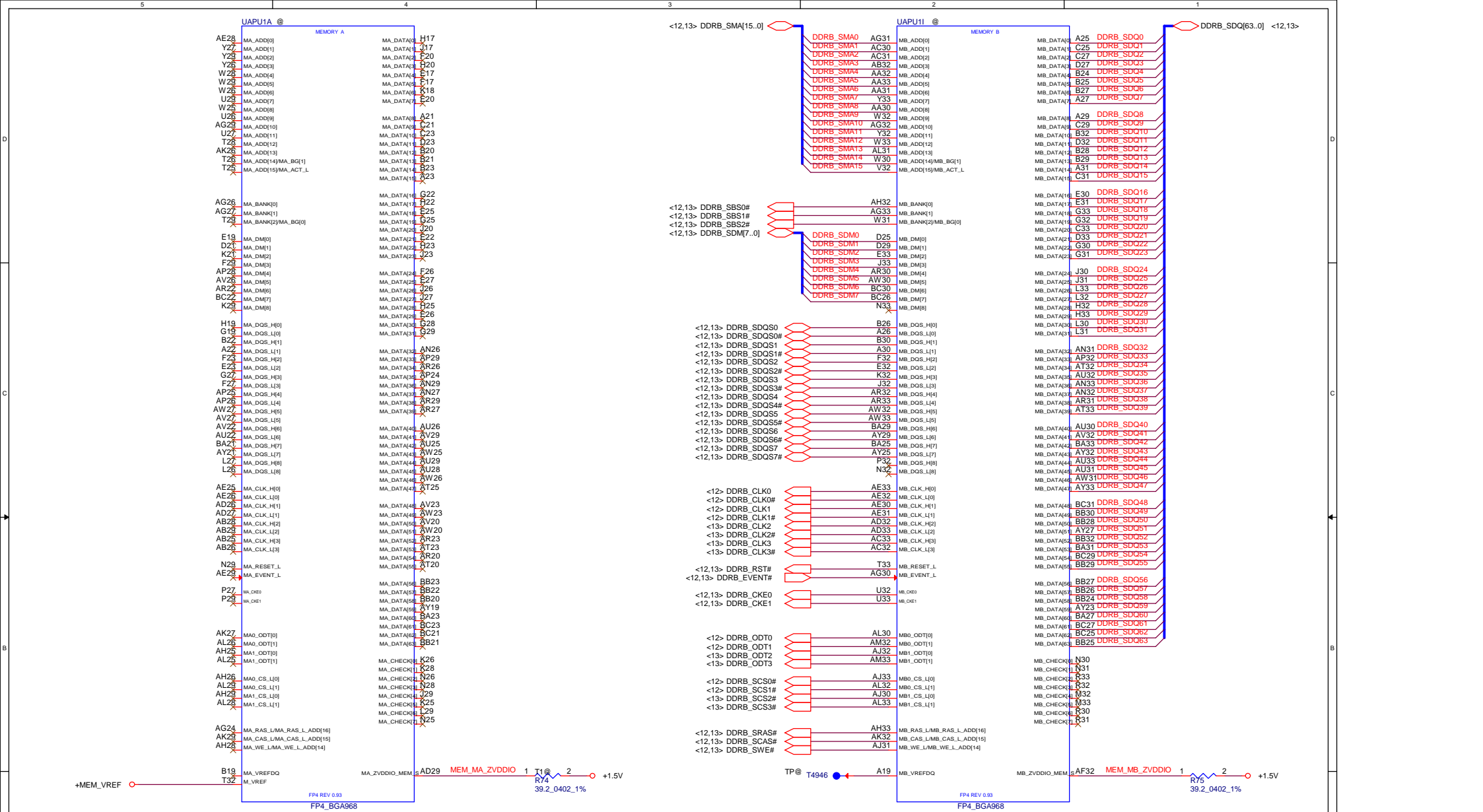
The waveforms show the following characteristics:

- +RTC:** A single high pulse.
- EC_ON:** A single high pulse.
- +5VALW:** A single high pulse.
- 3V_EN:** A single high pulse.
- +3VALW:** A single high pulse.
- 0.95_1.8VALW_PWREN:** A single high pulse.
- +1.8VALW/+0.95VALW:** A single high pulse.
- 0.95V_SPOK:** A single high pulse.
- +0.775VALW:** A single high pulse.
- SYSON:** A single high pulse.
- +1.5V:** A single high pulse.
- SUSP#:** A single high pulse.
- +5VS/+3VS/+1.8VS:** A single high pulse.
- +1.5VS/0.75VS:** A single high pulse.
- 0.95VS_PWR_EN#:** A single high pulse.
- +0.95VS:** A single high pulse.
- VR_ON:** A single high pulse.
- +APU_CORE:** A single high pulse.
- +APU_CORE_NB:** A single high pulse.
- +APU_GFX:** A single high pulse.

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	
4	
5	
6	
7	

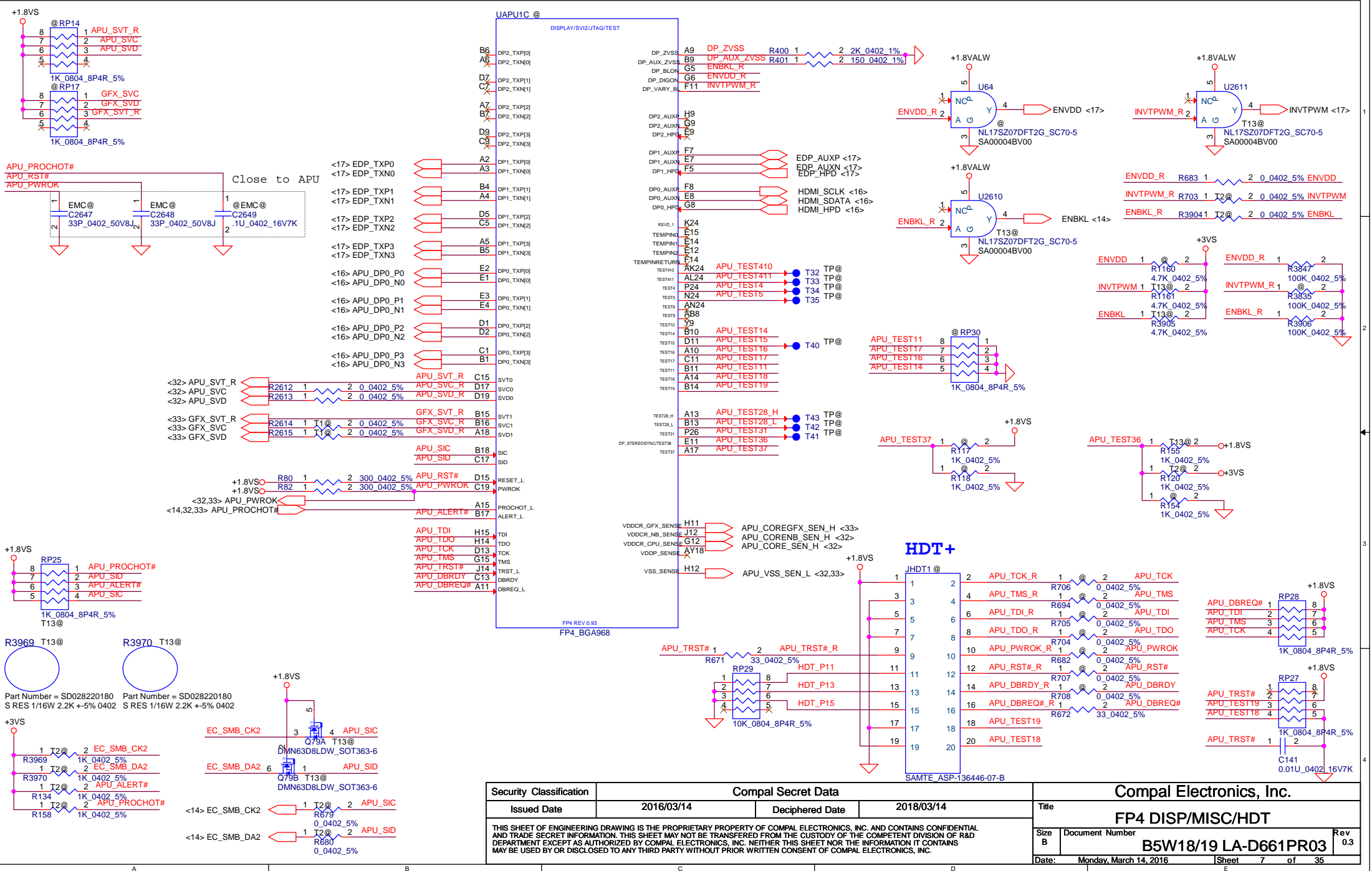
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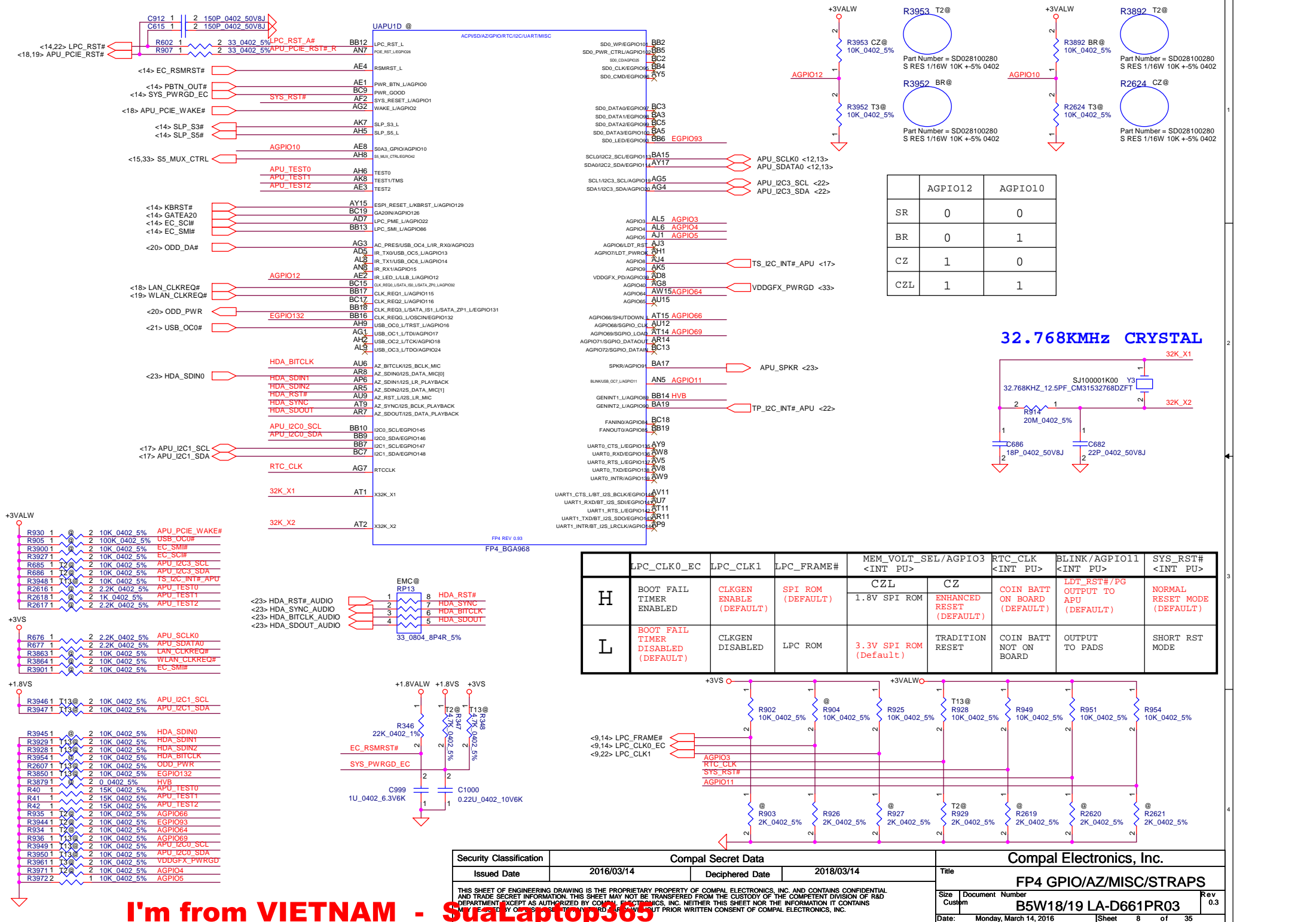


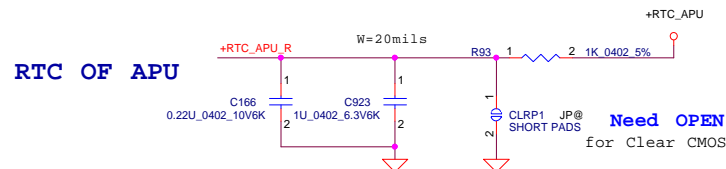
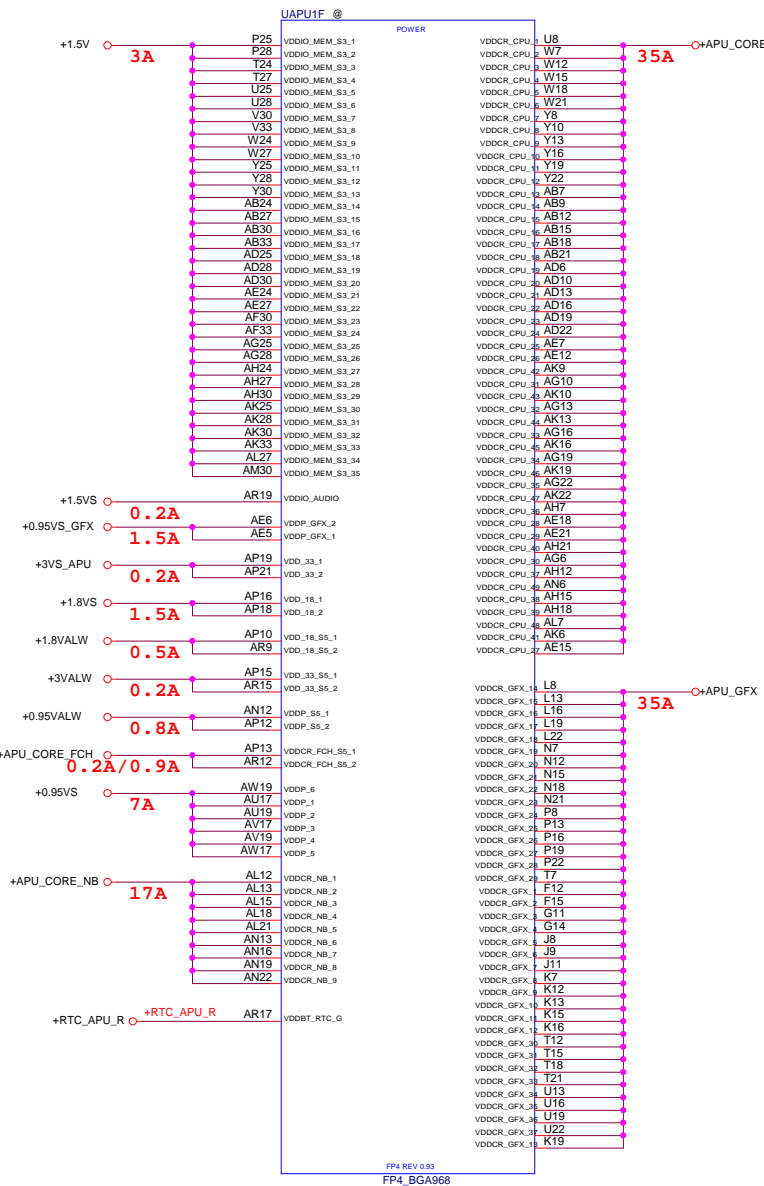
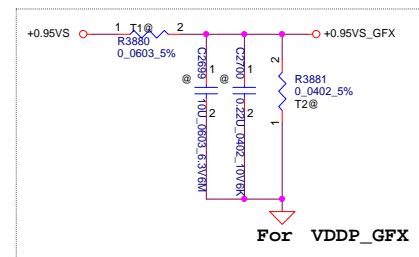
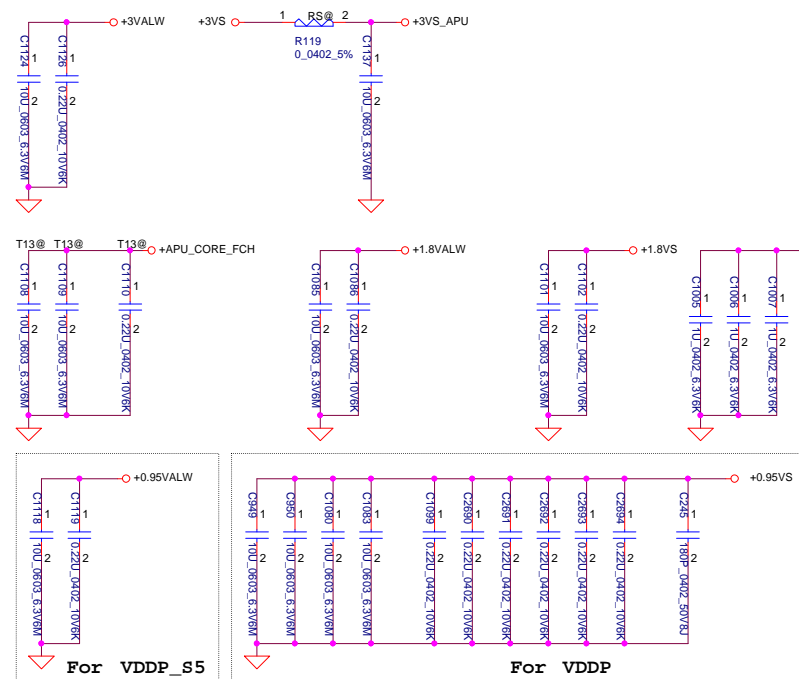
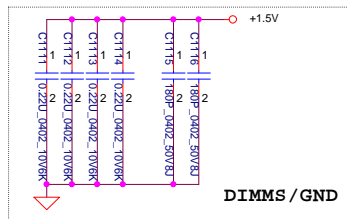
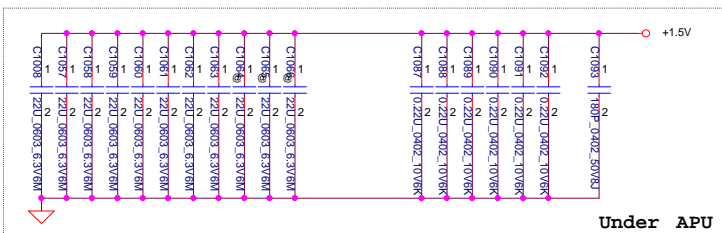
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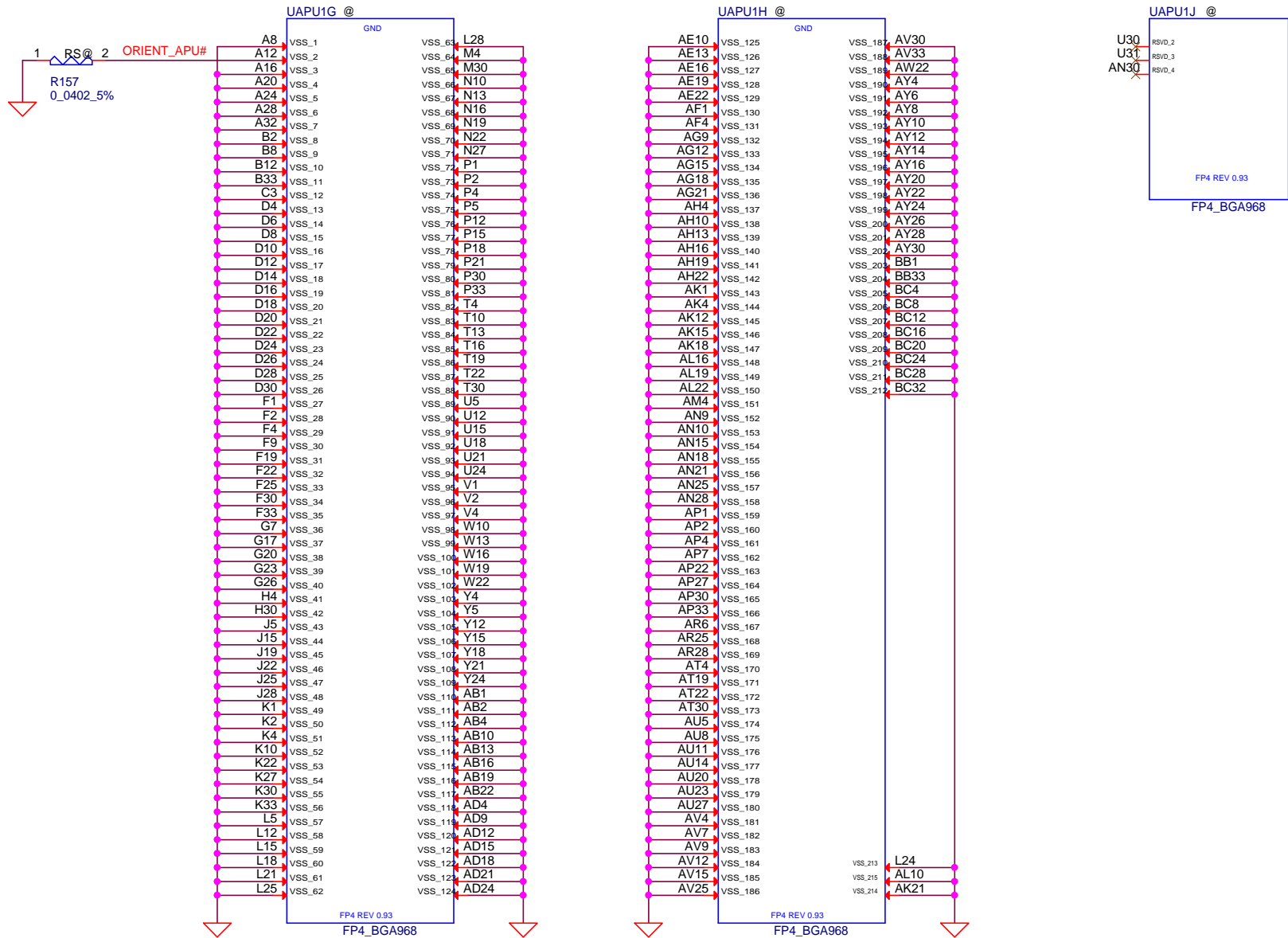
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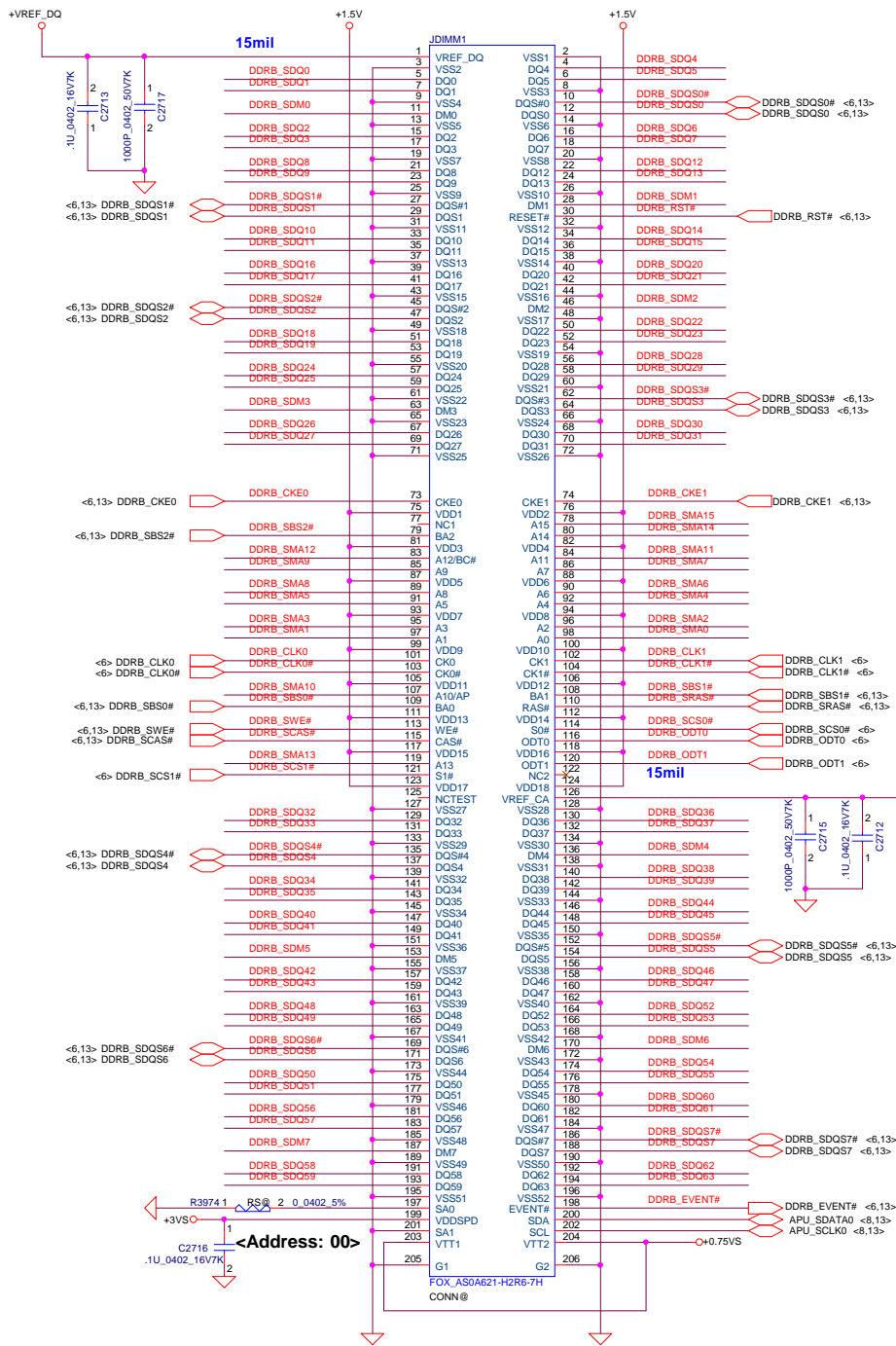
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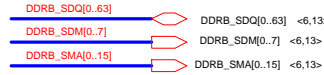


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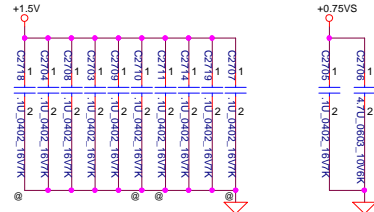
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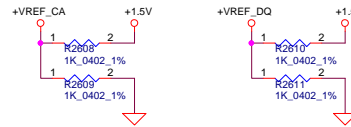
DIMM1 H:5.2mm RVS



+1.5V/+0.75V OF DIMM1

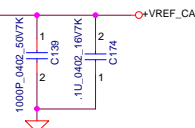
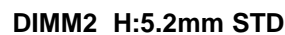


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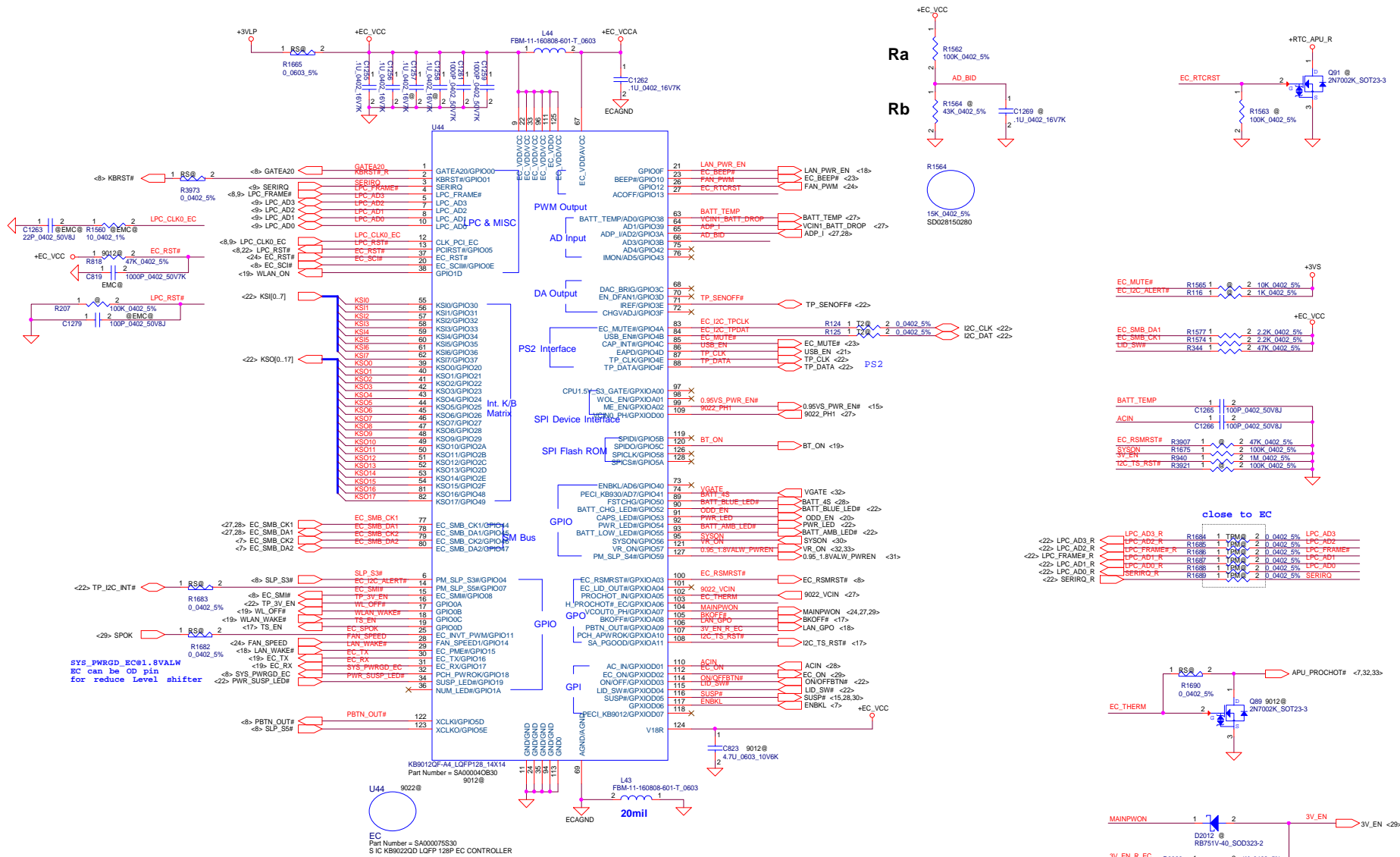


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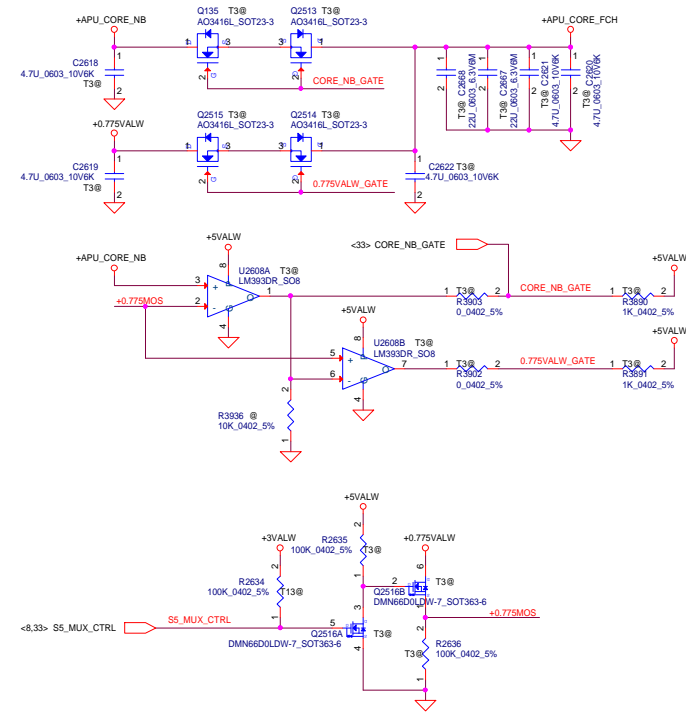
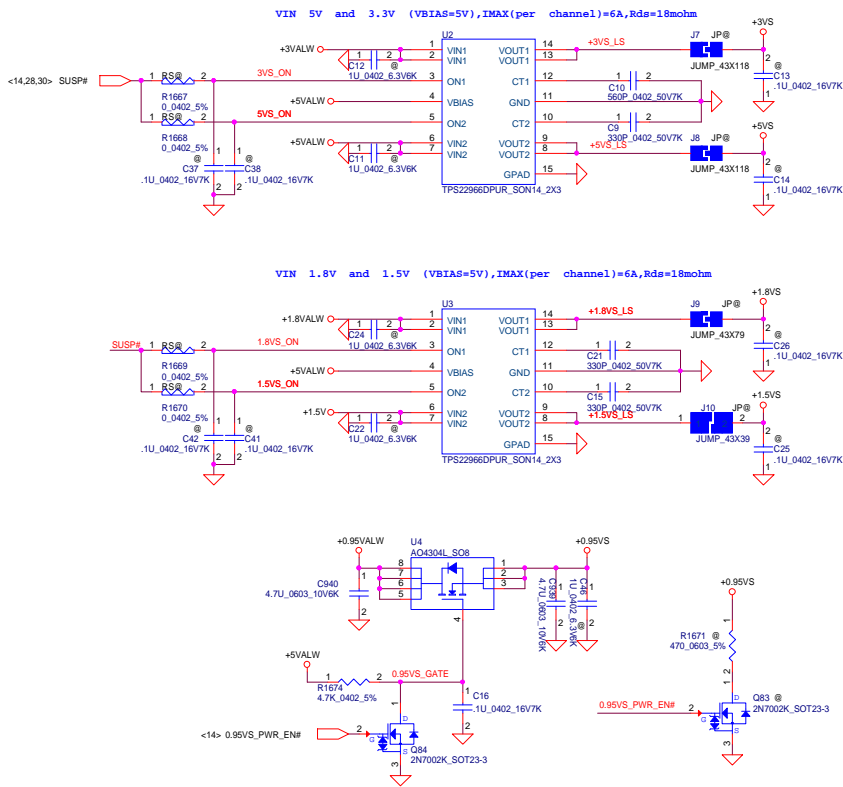


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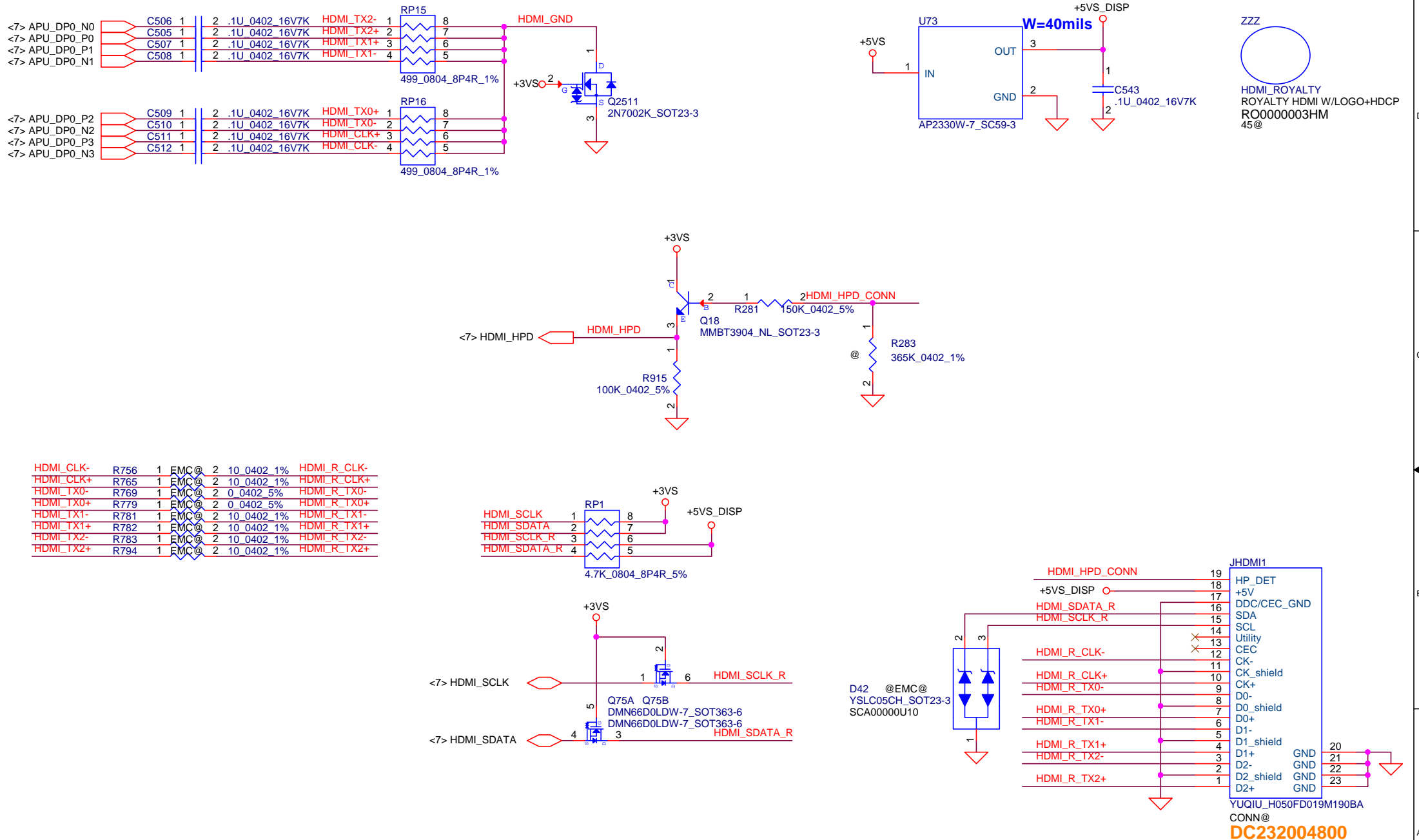
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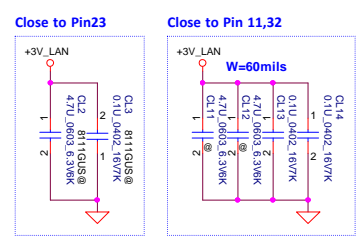
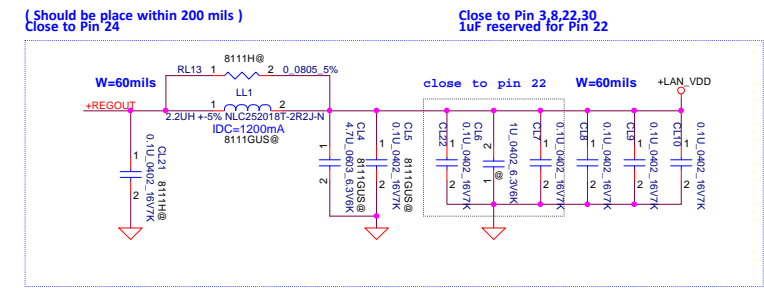
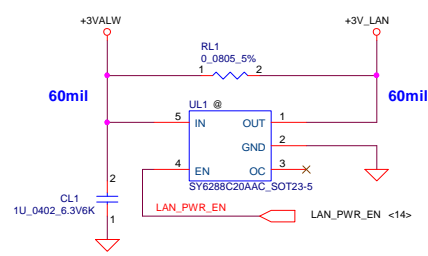
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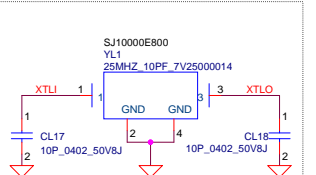
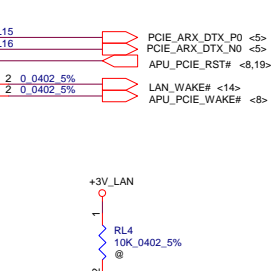
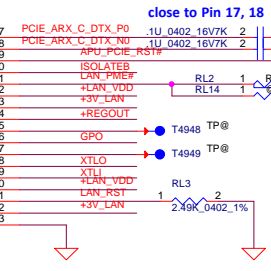
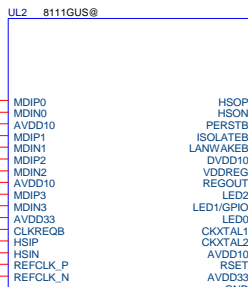
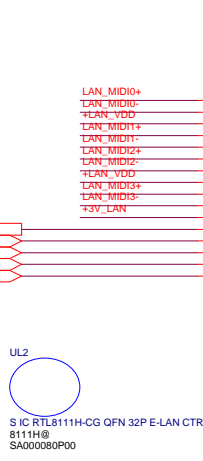
+3V_LAN Rising time request: 0.5~100 ns

SA000028Y10
High active
EN threshold voltage :1.2~2.0V
Current limit threshold :1.5~2.8A
Output turn-on rising time :1.3~2.7 ns

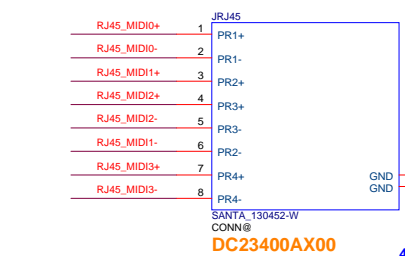
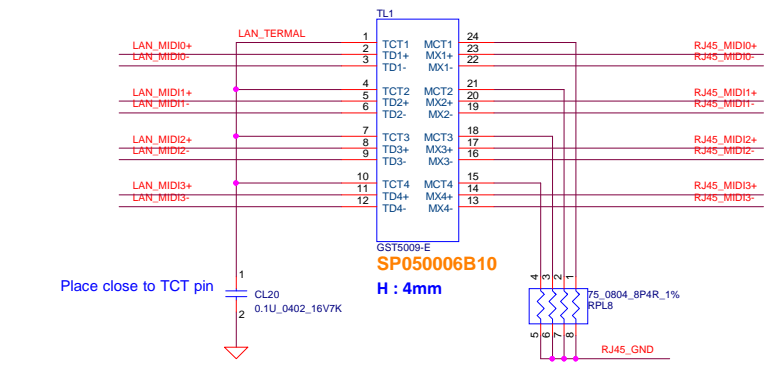
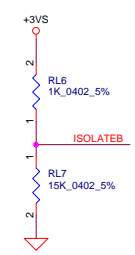


PU to +3VS at PCH side

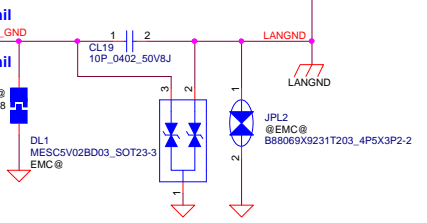
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<9> CLK_PCIE_LAN#



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.



LAN Connector



DC23400AX00

SP050006B10

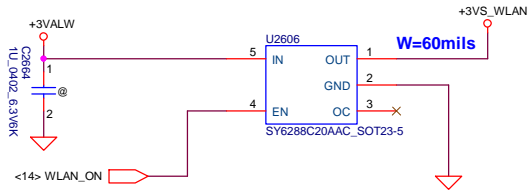
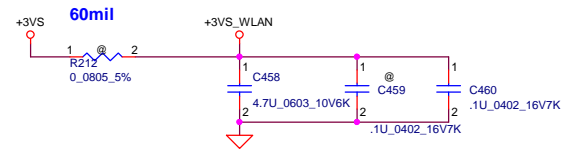
H : 4mm

Place close to TCT pin


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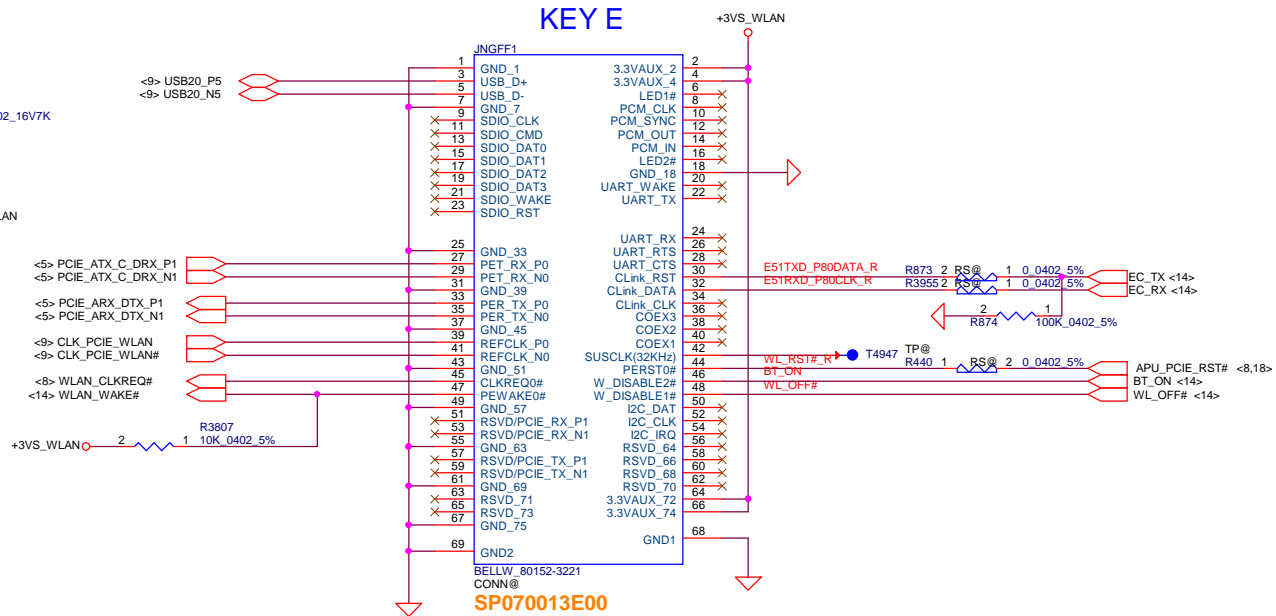
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Wireless LAN



NGFF WL+BT (KEY E)

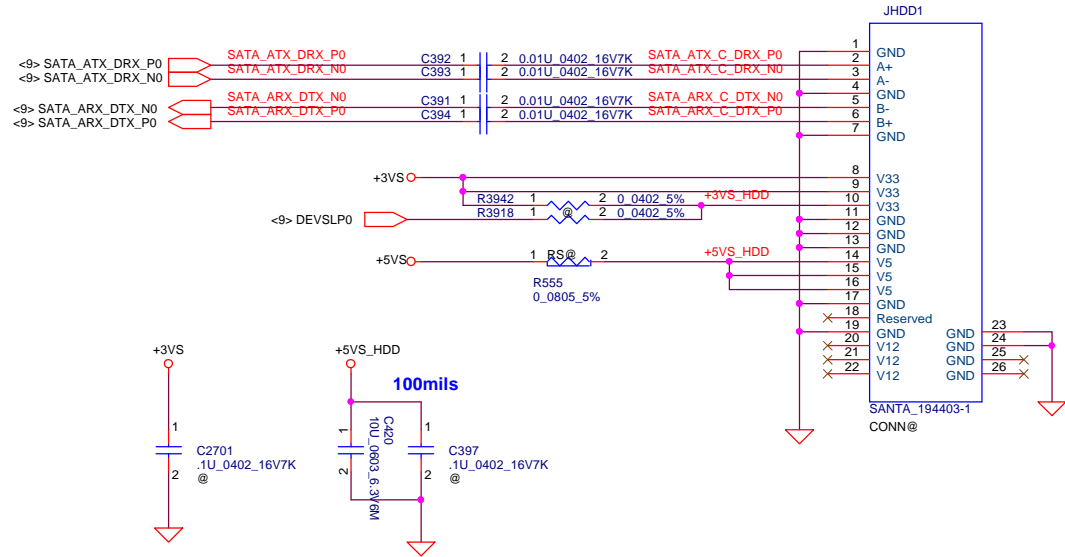
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLK1	73
70	UMI_Power_SMC(GPIO/PVAVoltd	RESERVED/REFCLKP1	71
68	UMI_Power_SMC/CLKREQID	GND	69
66	UMI_SWP/PERSTd	Reserved/PERn	67
64	Reserved	Reserved/PERp1	65
62	ALERTb (IO0/3.3)	GND	63
60	DC CLK (IO0/3.3)	Reserved/PETn1	61
58	DC DATA (IO0/3.3)	Reserved/PETp1	59
56	W_DISABLE1 (IO0/3.3)	GND	57
54	ReservedW_DISABLE1 (IO0/3.3)	PVAVoltd (IO0/3.3)	55
52	PERSTn (IO0/3.3)	CLKREQID (IO0/3.3)	53
50	SUSCLK32KHZ (IO0/3.3)	GND	51
48	CODEK1 (IO0/1.8V)	REFCLKn0	49
46	CODEK2 (IO0/1.8V)	REFCLKP0	47
44	CODEK3 (IO0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	PETn0	39
36	UART RTS (IO0/1.8V)	PETp0	37
34	UART CTS (IO0/1.8V)	GND	35
32	UART TX (IO0/1.8V)	GND	33
			RESERVED/REFCLK1 RESERVED/REFCLKP1 GND RESERVED/PERn RESERVED/PERp1 GND RESERVED/PETn1 RESERVED/PETp1 GND PVAVoltd (IO0/3.3) CLKREQID (IO0/3.3) GND REFCLKn0 REFCLKP0 GND PERn0 PERp0 PETn0 PETp0 GND
22	UART Rx (IO0/1.8V)	SIO0 Power (IO0/1.8V)	23
20	UART Wakeup (IO0/3.3)	SIO0 Wakeup (IO0/1.8V)	21
18	GND	SIO0 DATA TX (IO0/1.8V)	19
16	LED1d (VIO0)	SIO0 DATA TX (IO0/1.8V)	17
14	PCM_IN/VS2_OUT (IO0/1.8V)	SIO0 DATA TX (IO0/1.8V)	15
12	PCM_IN/VS2_IN (IO0/1.8V)	SIO0 DATA TX (IO0/1.8V)	13
10	PCM_SYNC/VS1 (IO0/1.8V)	SIO0 CM0 (IO0/1.8V)	11
8	PCM_CLK/VS2/CLK (IO0/1.8V)	SIO0 CLK0 (IO0/1.8V)	9
6	LED1d (VIO0)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3



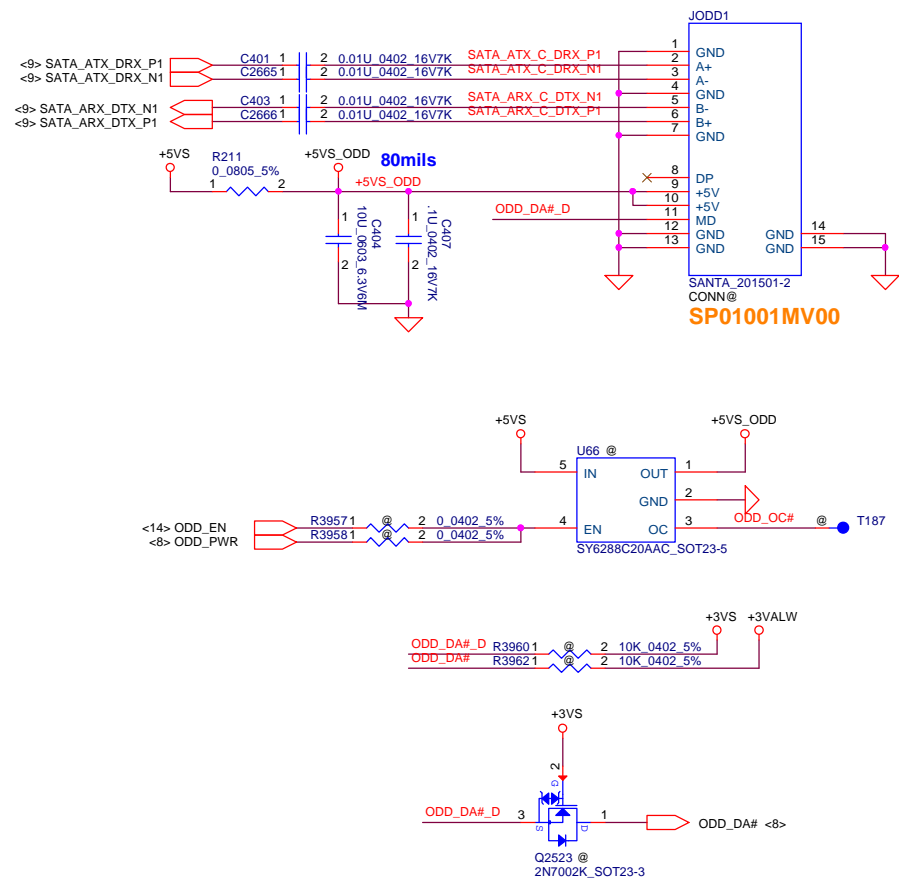
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SATA HDD Conn.

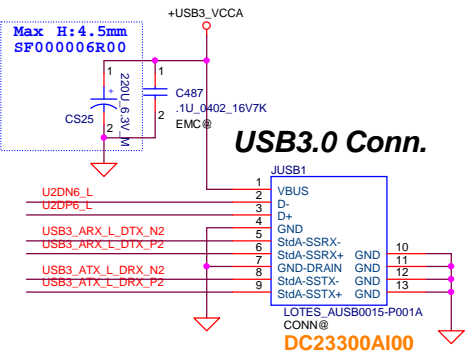
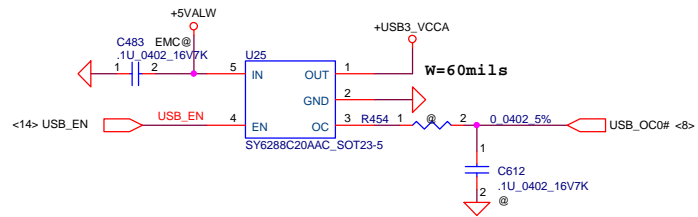
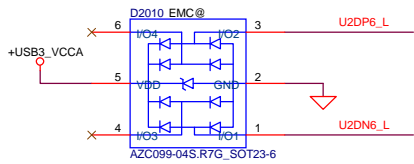
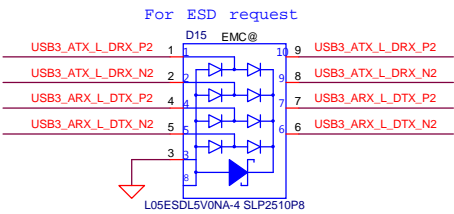
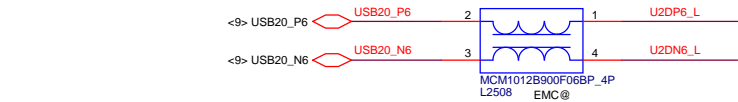
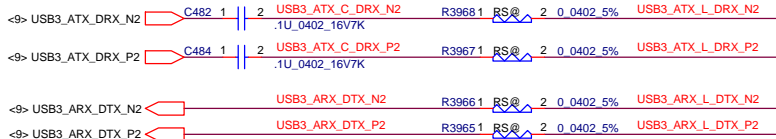


SATA ODD Conn.

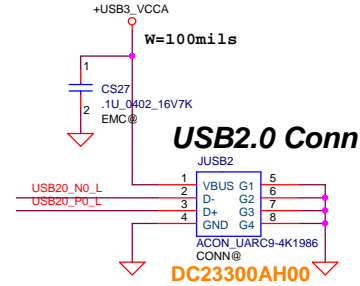
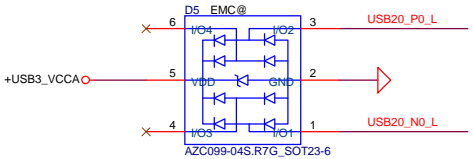
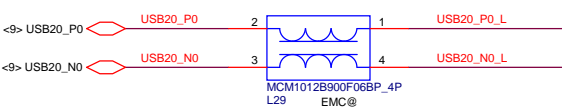


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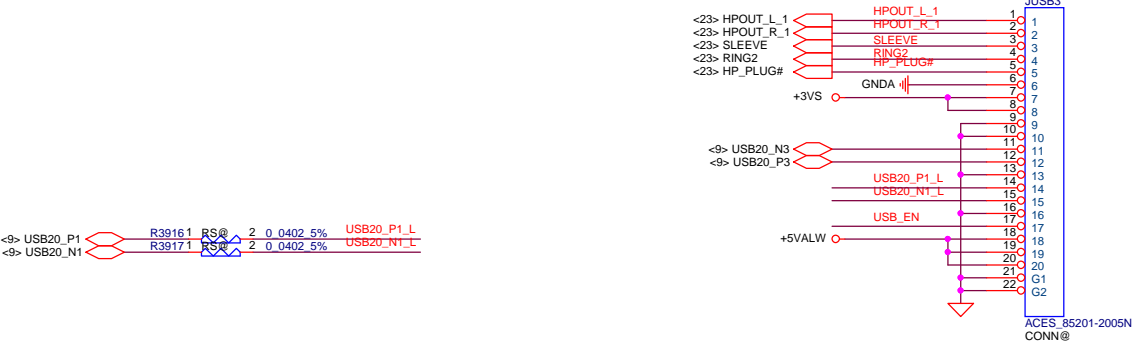
USB3.0 (Port 2)



USB2.0 (Port 0)



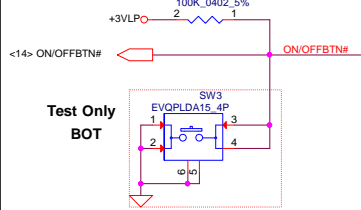
USB/B (USB, AUDIO, CR)



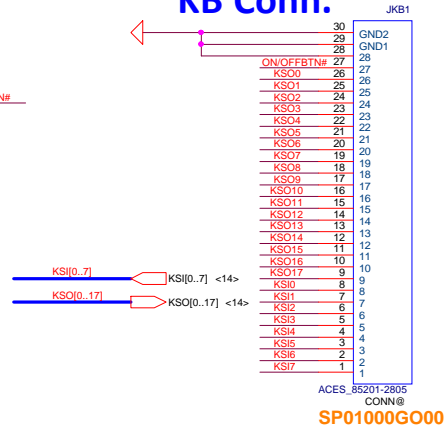
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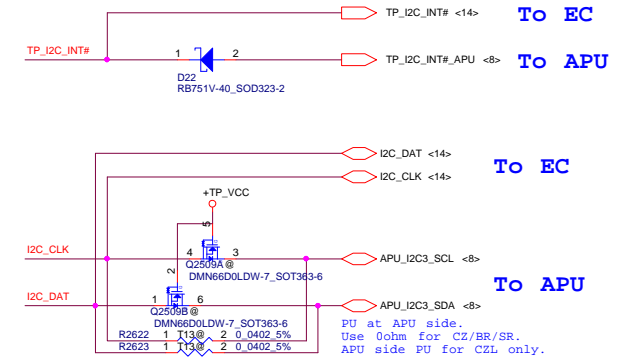
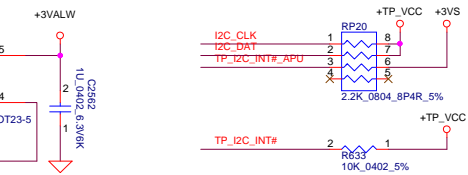
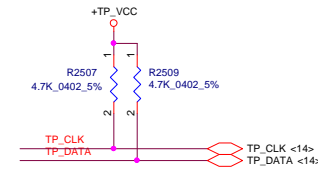
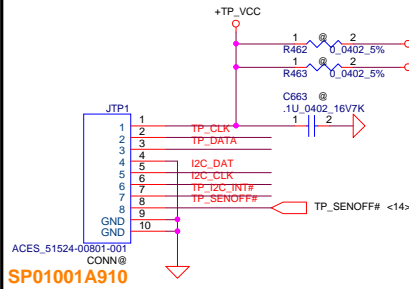
ON/OFF BTN



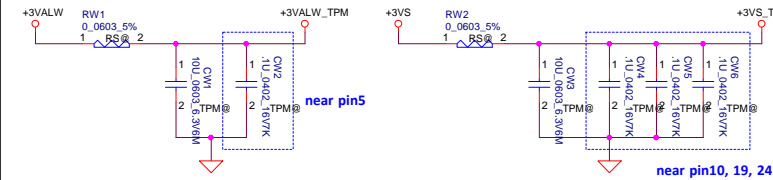
KB Conn.



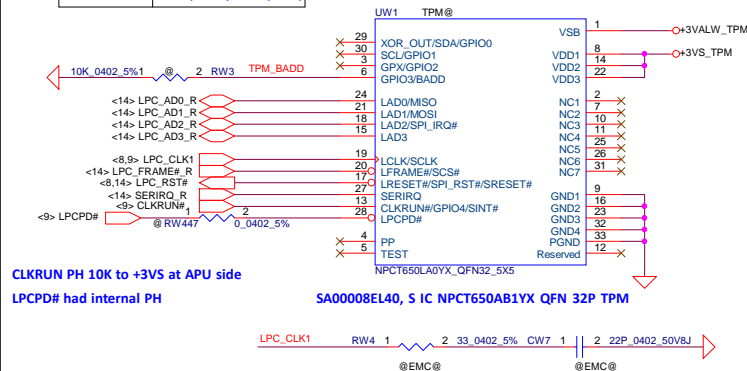
TP/B Conn.



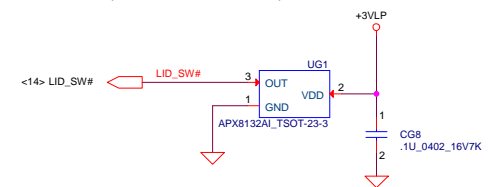
TPM



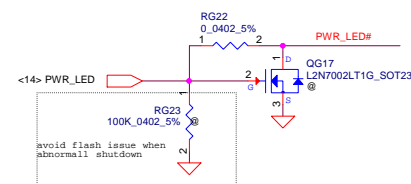
BADD	SELECTION
* 1	AEh(write), AFh(read)



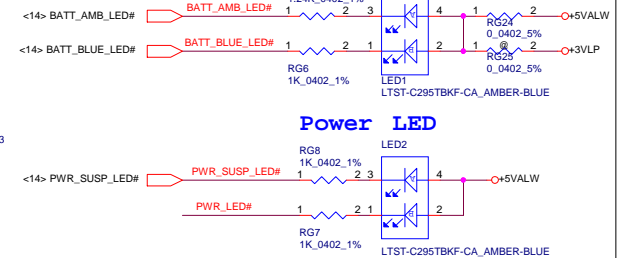
Lid Switch (Hall Effect Switch)



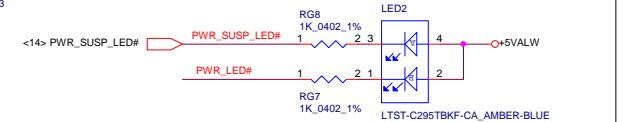
LED



Battery LED



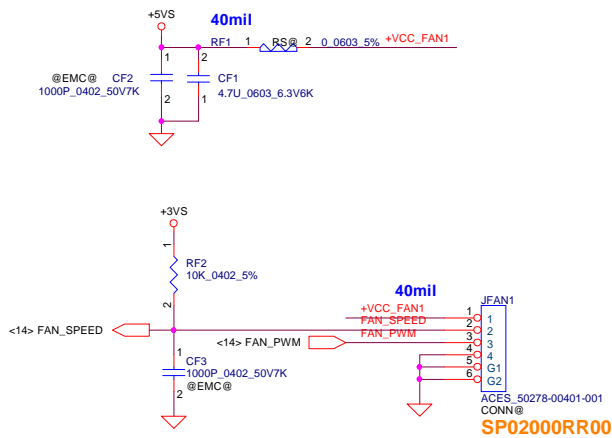
Power LED



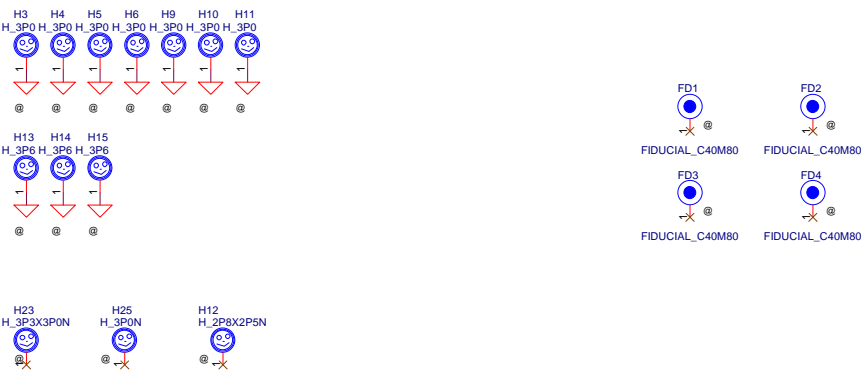
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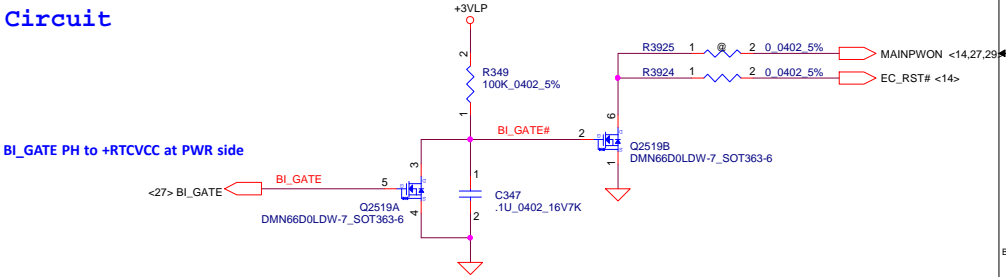
FAN Conn



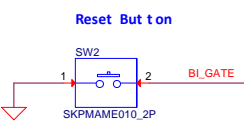
Screw Hole



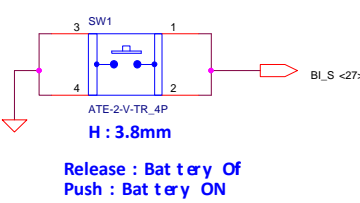
Reset Circuit



Reset But t on



BI SW

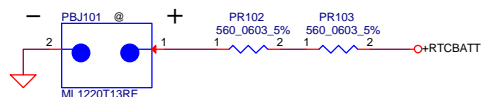
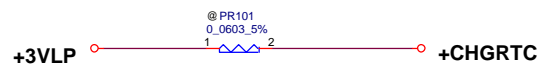
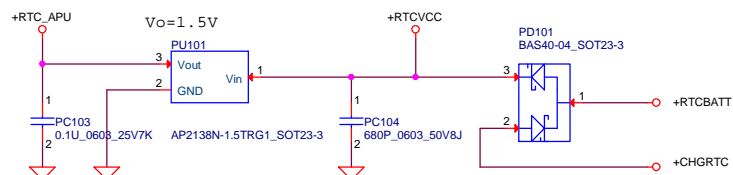
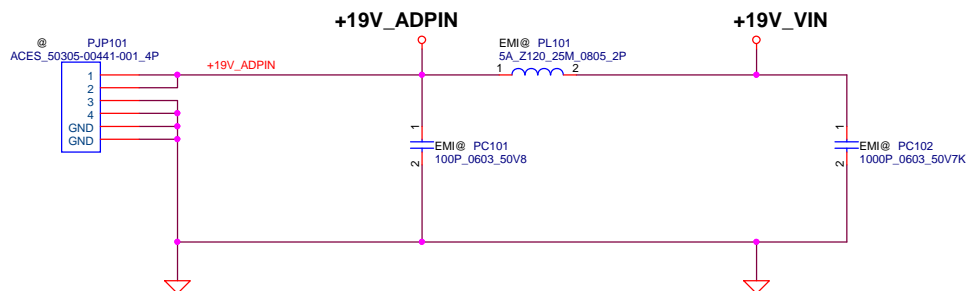


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- 0.2
- 1. Change EC BID to 1 for DVT,R1564 change to 12Kohm.
 - 2. Change R756,R765,R781,R782,R783,R794 to 10 ohm for HDMI EA result.
 - 3. Combine power.
 - 4. Change R555,RL2,RL5 to R-short;Unpop R682,R694,R704,R705,R706,R707,R708.
 - 5. Change H13,H14,H15 to H_3P6.
 - 6. Combine power.
 - 7. Combine power.
 - 8. Combine power.
 - 9. Change C2647,C2648 to 33P for ESD request.
 - 10. Pop R1562 for EC BID to 1.
 - 11. Change RG4 to 1.24kohm; RG6,RG7,RG8 to 1kohm.
- 0.3
- 1. Change R108,R3916,R3917,R3963,R3964,R3965,R3966,R3967,R3968,R873,R3955 to R-short.
 - 2. Change EC BID to 2 for PVT,R1564 change to 15Kohm.
 - 3. Combine power.

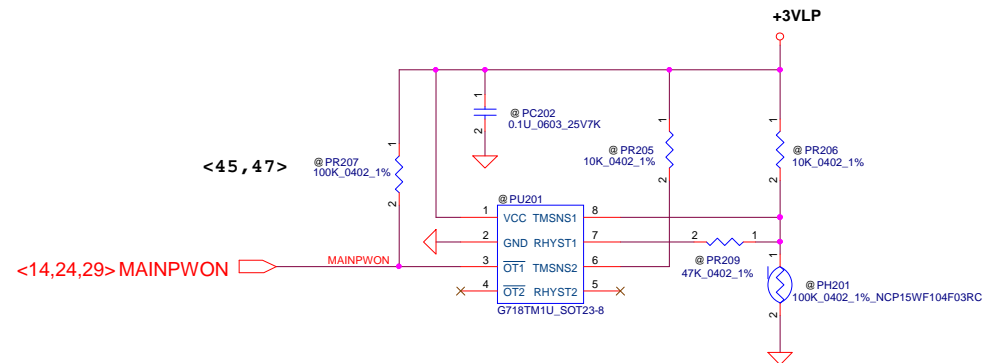
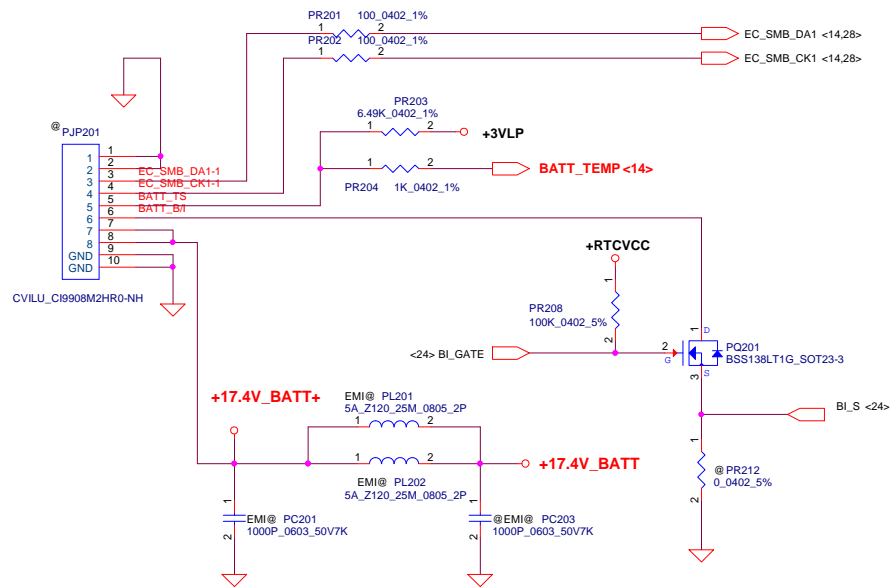
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					HW-PIR		
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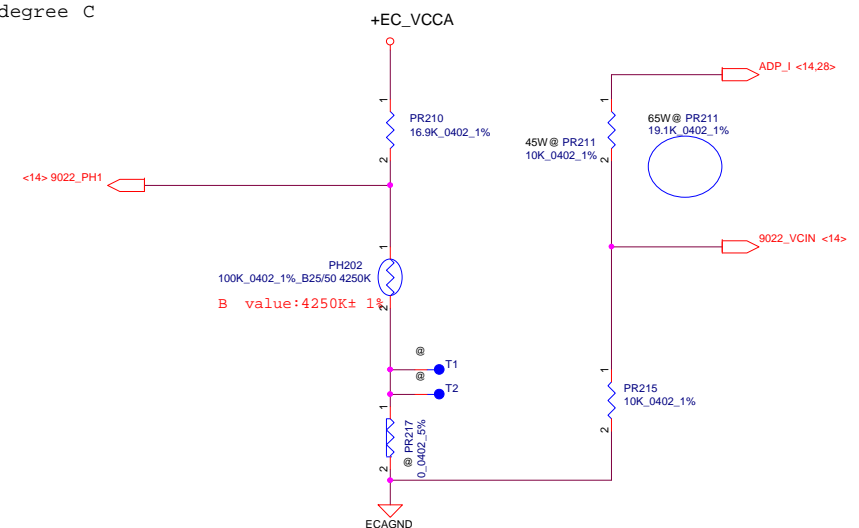
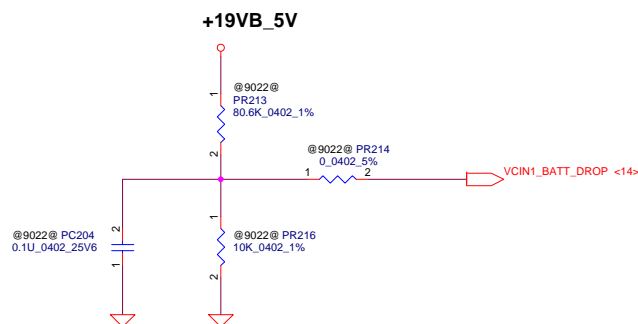
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3092K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

PH202 under CPU bottom side :
 CPU thermal protection at 96 degree C (shutdown)
 Recovery at 56 degree C

2013/10/02
 Add for ENE9022 Battery Voltage drop detection.
 Connect to ENE9022 pin64 AD1.

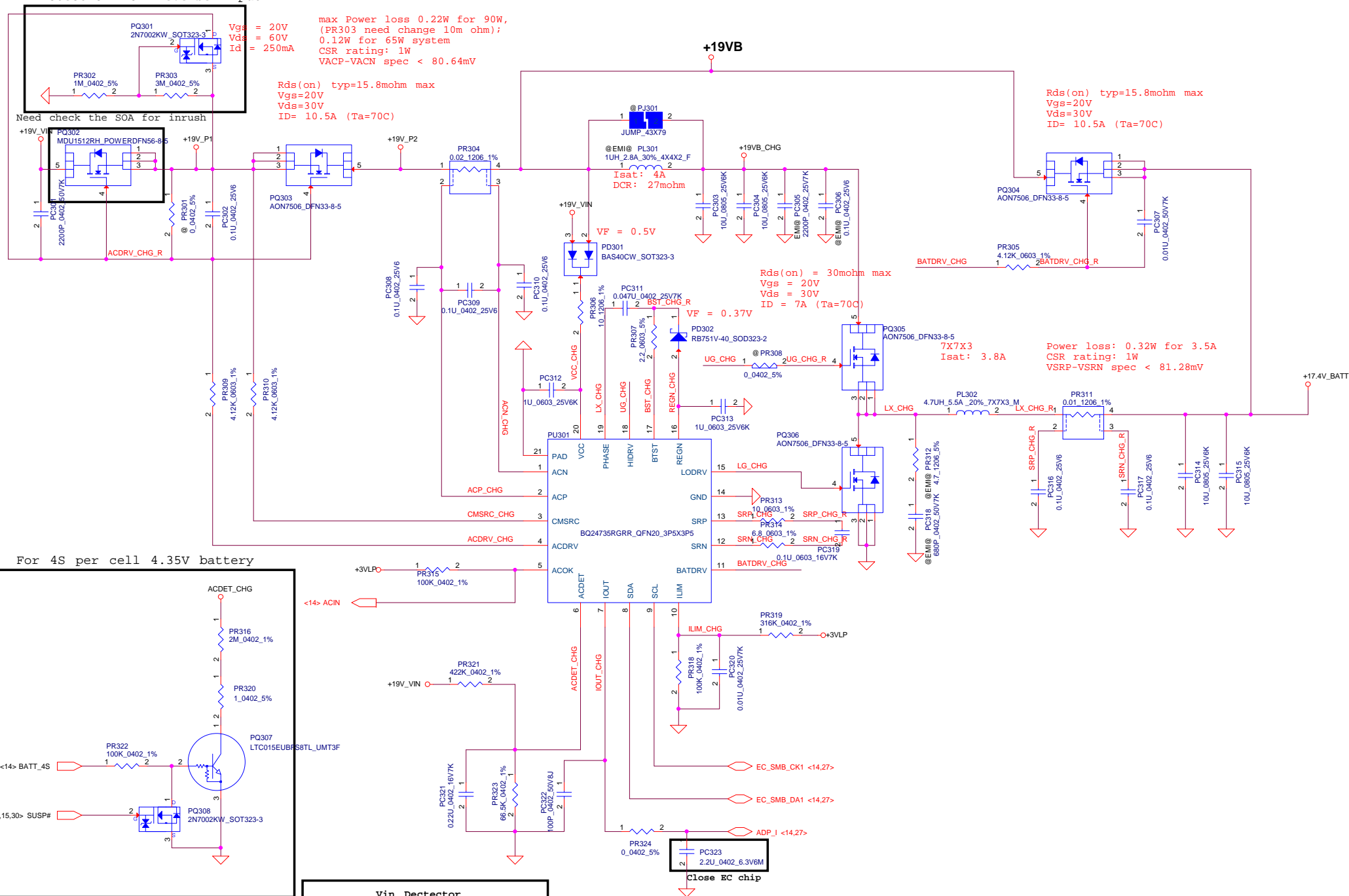
Reserve for 2-cell design



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Protection for reverse input



	Vin Dectector		
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$$\begin{aligned} \text{VILIM} &= 20 \cdot \text{ILIM} \cdot \text{Rsr} \\ \text{ILIM} &= 3.3 \cdot 100 / (100 + 316) / 20 / 0.01 \\ &= 3.966 \text{ A} \end{aligned}$$

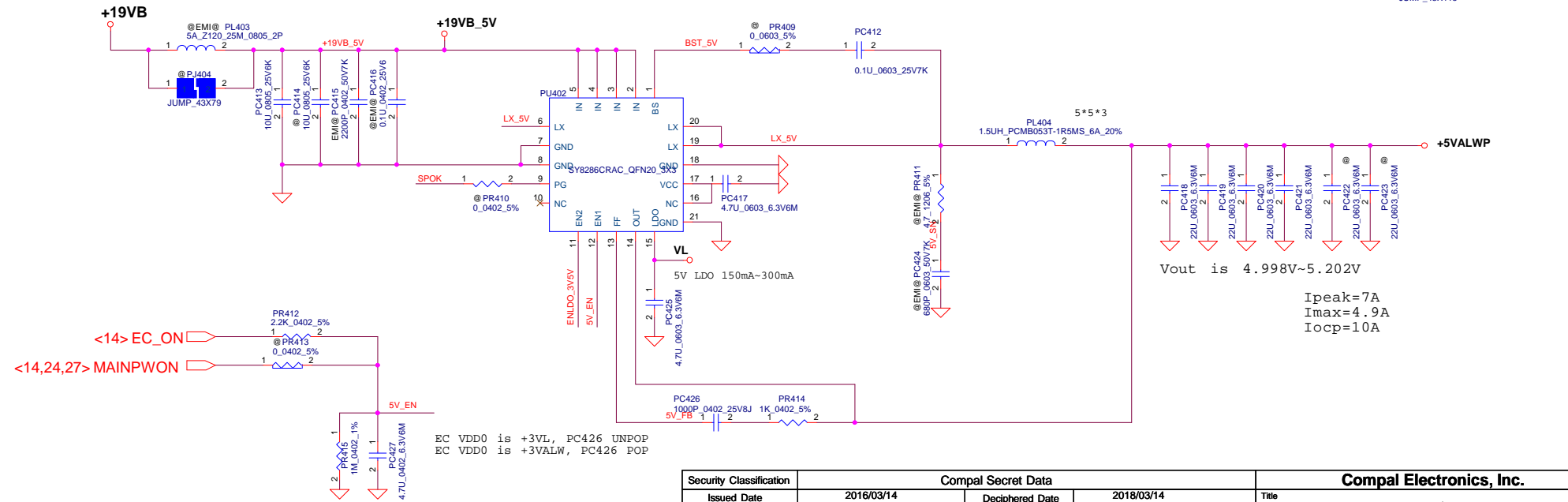
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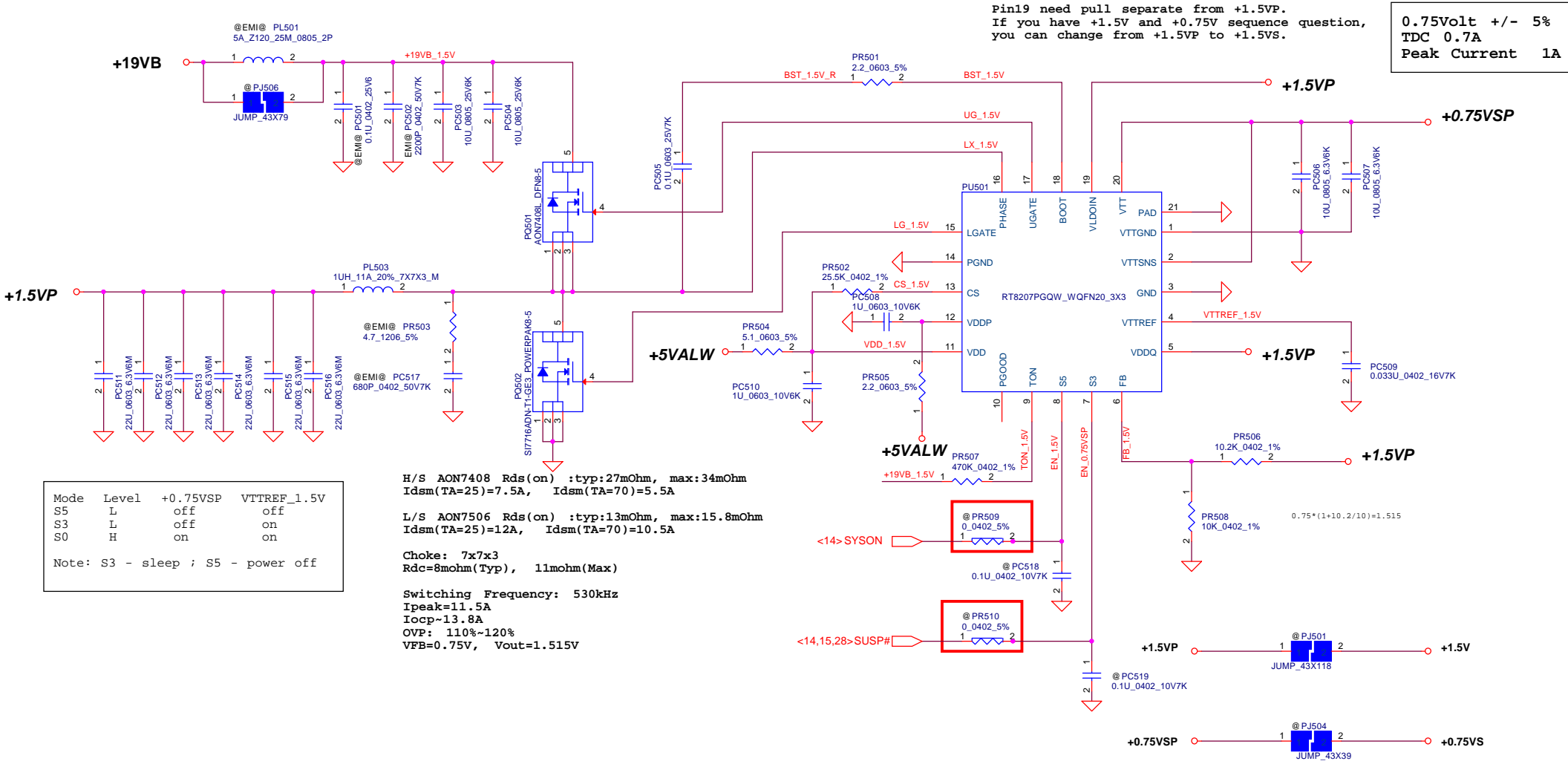
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Check pull up resistor of
SPOK at HW side



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Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

H/S AON7408 Rds(on) :typ:27mOhm, max:34mOhm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13mOhm, max:15.8mOhm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

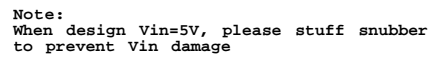
Choke: 7x7x3
Rdc=8mohm(Typ), 11mohm(Max)

Switching Frequency: 530kHz
Ipeak=11.5A
IoCP=13.8A
OVP: 110%~120%
VFB=0.75V, Vout=1.515V

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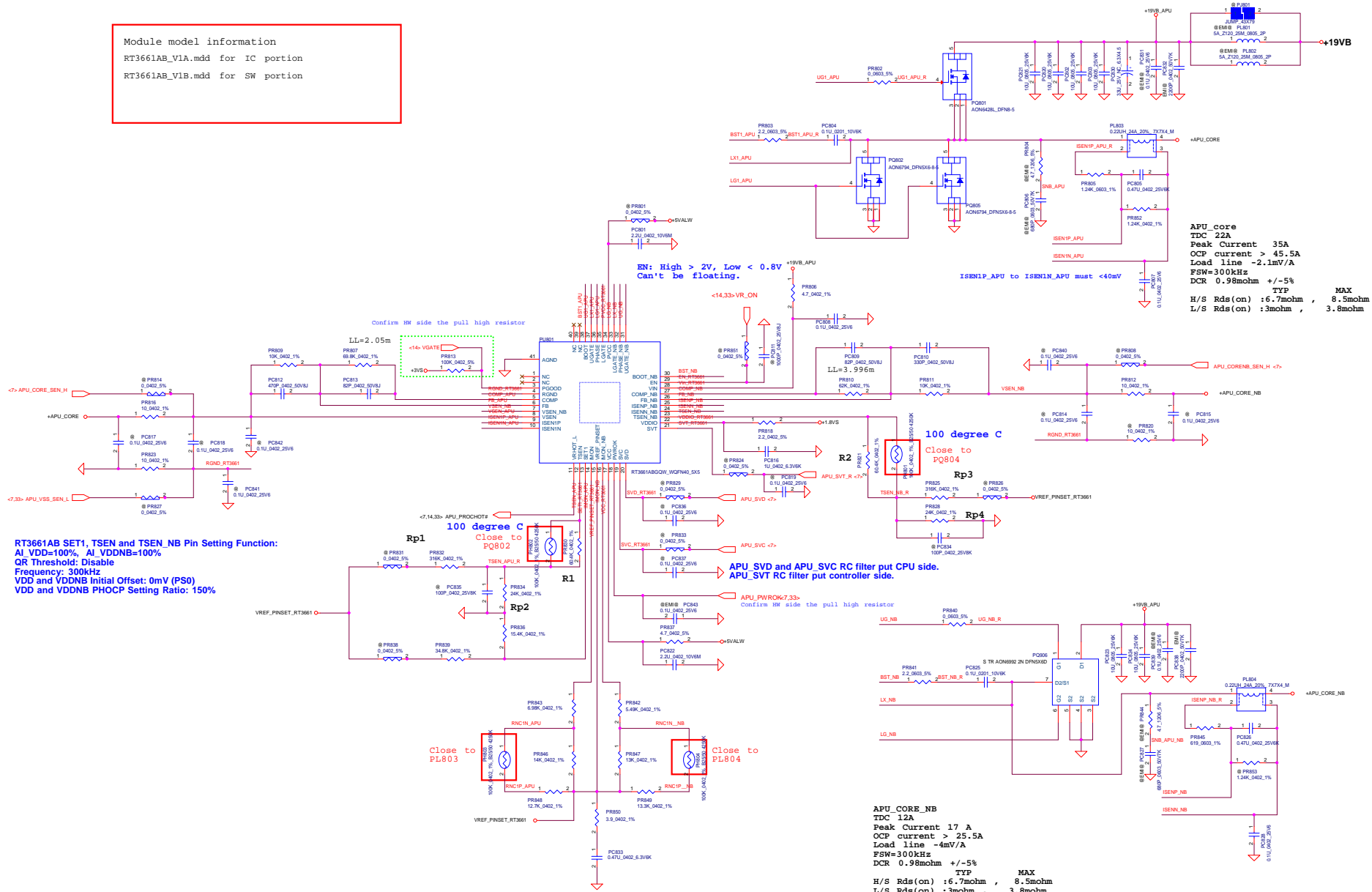
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Module model information
SY8208D_V1.mdd
```



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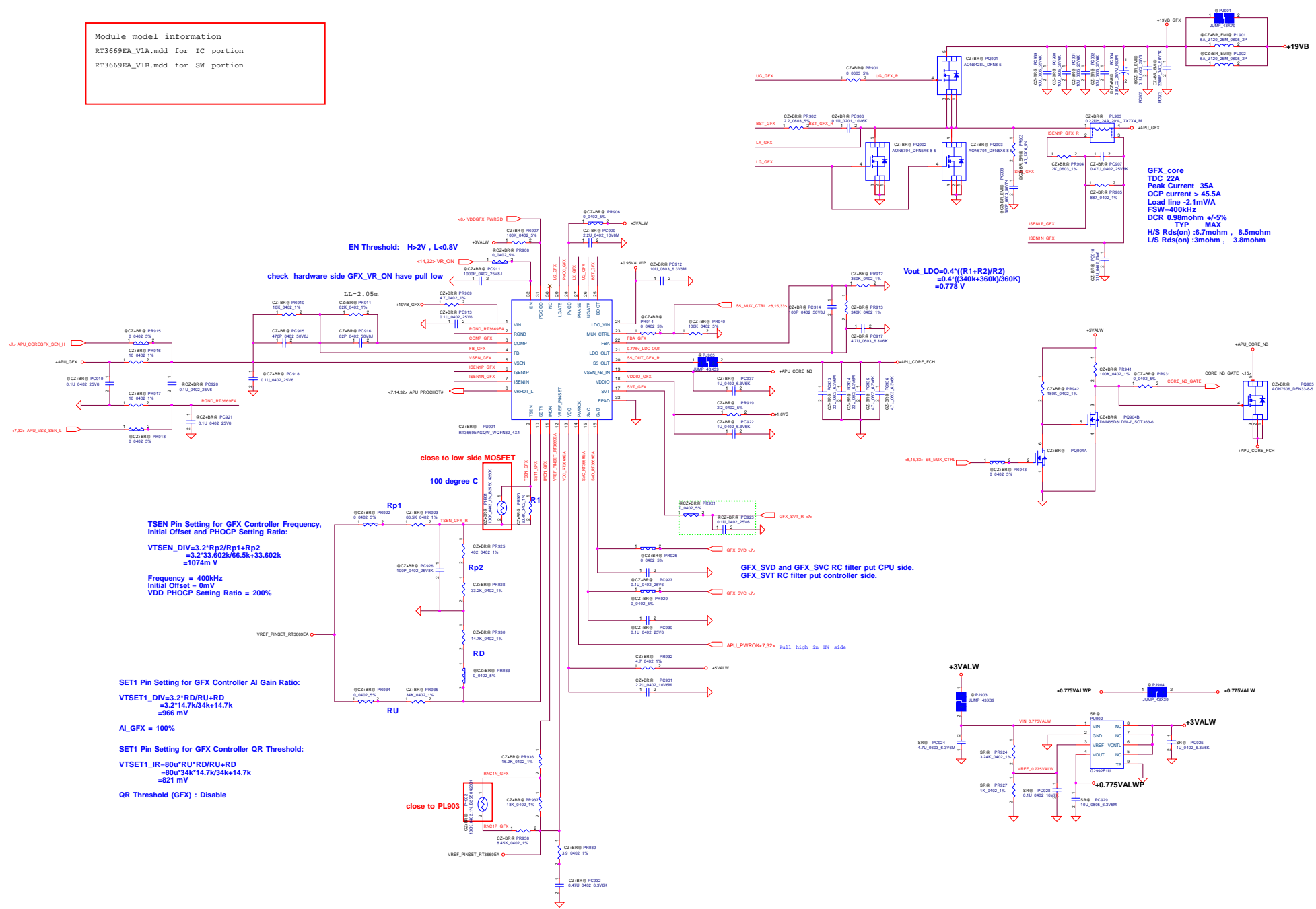
Module model information
RT3661AB_V1A.mdd for IC portion
RT3661AB_V1B.mdd for SW portion



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Module model information
RT3669EA_V1A.mdd for IC portion
RT3669EA_V1B.mdd for SW portion
```



GFX_core
TDC 22A
Peak Current 35A
OCP current > 45.5A
Load line -2.1mV/A
FSW=400kHz
DCR 0.98mohm +/-5%
TYP MAX
H/S Rds(on) :6.7mohm , 8.5mohm
L/S Rds(on) :3mohm , 3.8mohm

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+APU_CORE

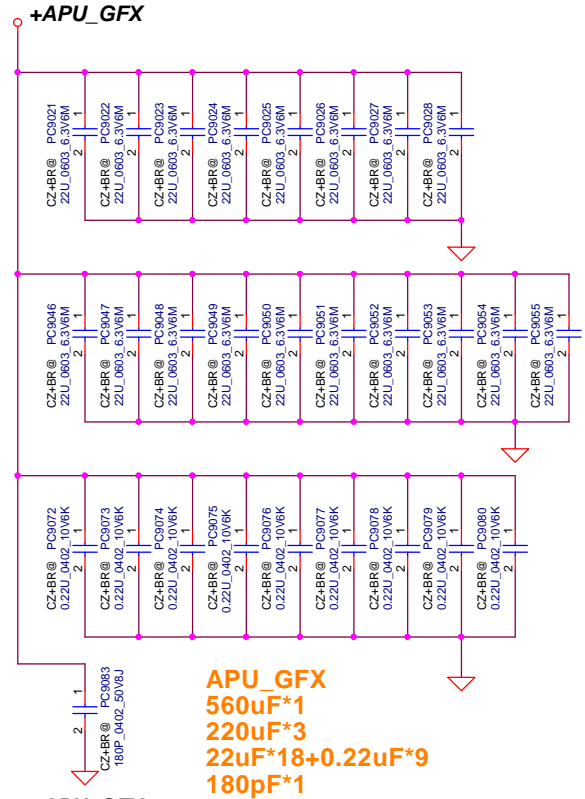
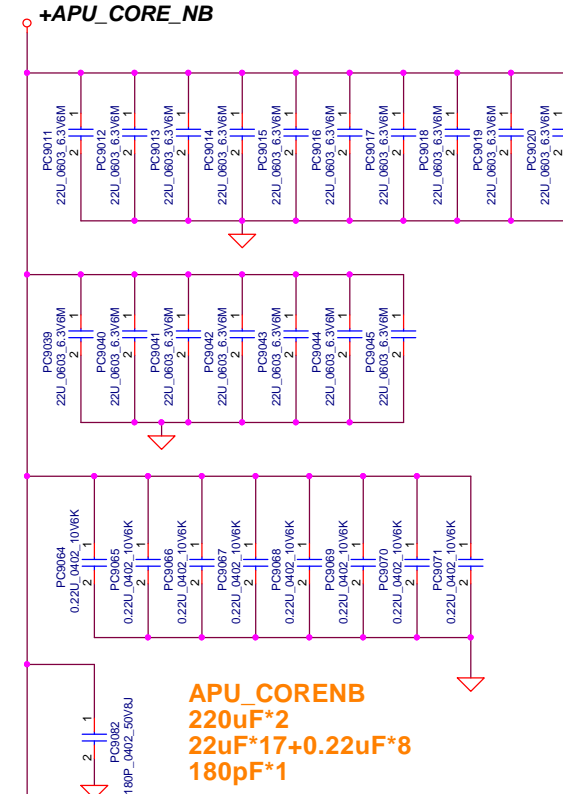
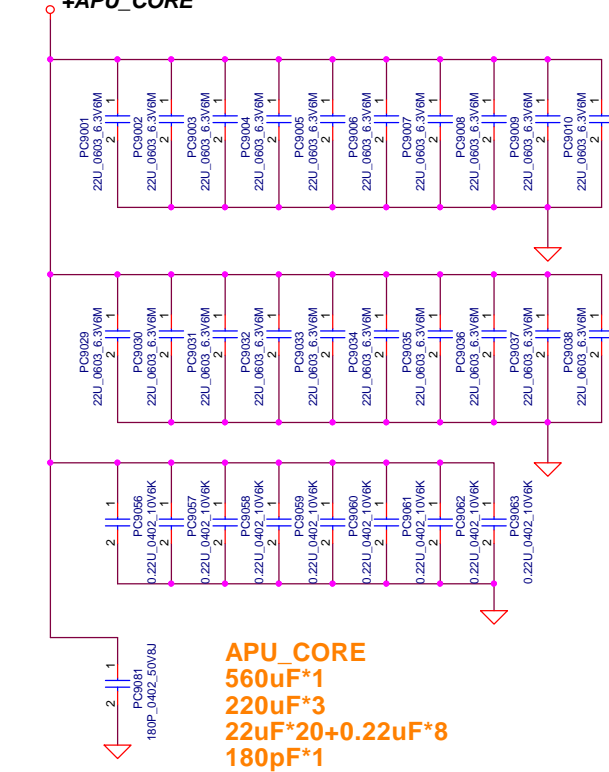
+APU_CORE_NB

+APU_GFX

+APU_CORE

+APU_CORE_NB

+APU_GFX



change PC9088 from
SGA20221D40 (220u) to
SGA00009S00 (330u)
(common part)

PC9088
330U_D2_2V_V_Y

PC9089
220U_D2_SX_2V_V_R9M

CZ4BR@ PC9093
220U_D2_SX_2V_V_R9M

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	electrolytic capacitor is close to PCB edge, high risk of component crack issue.	electrolytic capacitor is close to PCB edge, high risk of component crack issue.	01	33	change PC904 to SGA00007I00 for DFB request		
02	tune CPU transient and LL	tune CPU transient and LL	01	32 33	change PC810 from 470p to 330p change PR807 from 64.9k to 69.8k change PR810 from 59k to 62k change PR911 from 64.9k to 82k change PC9091from SGA20221D40 to SF000008L00 change PC9088 from SGA20221D40 (220u) to SGA00009S00 (330u) (common part) unpop PC9084, PC9086, PC9089, PC9092, PC9093		
03	in S5, APU_CORE_FCH leakage to APU_CORE_NB	in S5, APU_CORE_FCH leakage to APU_CORE_NB	01	33	unpop PQ905 add PR931 0ohm and connect to CORE_NB_GATE		
04	reduce part count	reduce part count	01	32 33	change 0ohm to R-short: PR918, PR933, PR833, PR926, PR929, PR814, PR943, PR824, PR908, PR801, PR851, PR914, PR808, PR826, PR922, PR838, PR906, PR827, PR934, PR829, PR831, PR921, PR915		
05							
06							
07							
08							

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